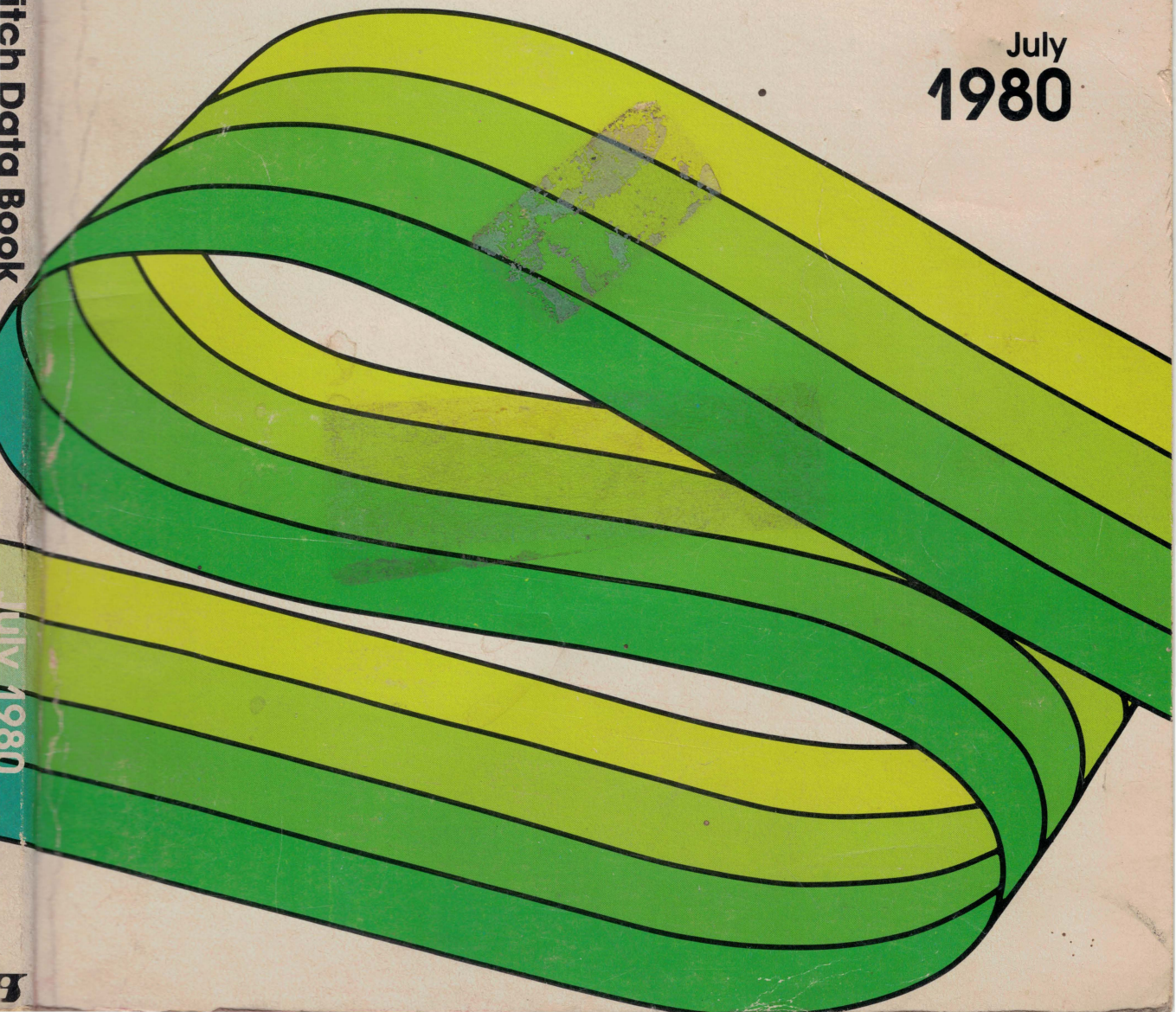
Siliconix

Analog Switch Data Book

July 1980



Siliconix Analog Switch Data Book July 1980

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Contents

How to Use 0-3
Cross Reference/Substitution Guide Integrated Circuits 0-5
Product Selector Guide by Applications 0-8
Typical Performance Characteristics 0-11
Preferred Product Selector Guide 0-12
Process Option Flow Chart 0-14
JAN 38510 Analog Switches 0-16
JM38510/883 Process Option Flow Chart 0-17
BS9000 Approved Analog Switches 0-18
BS9000 Series Process Option Flow Chart 0-19
BS9000 Approved Parts 0-20
Device Ordering Information 0-21

ANALOG SWITCHES INDEX 1

See Numeric-Alpha Index, page 0-2

DRIVERS FOR FET SWITCHES INDEX 2

See Numeric-Alpha Index, page 0-2

MULTI-CHANNEL FETs INDEX 3

See Numeric-Alpha Index, page 0-2

DIE PROCESS AND TOPOGRAPHY INFORMATION INDEX 4

See Numeric-Alpha listing on Index 4 title page.

BURN-IN PIN CONNECTIONS INDEX 5

MECHANICAL DATA INDEX 6

APPENDICES INDEX 7

Publications Index 7-1
Glossary of Terms and Abbreviations 7-3
Sales Offices 7-5

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Numeric-Alpha Index

TYPE #		PAGE
DGM	111	1-1
G	115	3-1
G	116	3-3
G	117	3-5
G	118	3-7
G	119	3-9
DGM	122	1-4
G	122	3-11
D	123	2-1
DG	123	1-7
G	123	3-13
D	125	2-3
DG	125	1-10
DG	126	1-13
D	129	2-5
DG	129	1-16
DG	133	1-16
DG	134	1-13
D	139	2-7
DG	139	1-19
DG	140	1-22
DG	141	1-22
DG	142	1-25
DG	143	1-25
DG	144	1-19
DG	145	1-28
DG	146	1-28
DG	151	1-31
DG	152	1-34
DG	153	1-31
DG	154	1-34
DG	161	1-37
DG	162	1-40
DG	163	1-37
DG	164	1-40
DG	172	1-43
DG	180	1-46
DG	181	1-46
DG	182	1-46

TYPE #		PAGE
DG	183	1-46
DG	184	1-46
DG	185	1-46
DG	186	1-46
DG	187	1-46
DG	188	1-46
DG	189	1-46
DG	190	1-46
DG	191	1-46
DG	200	1-52
DG	201	1-59
DG	211	1-66
DG	281	1-68
DG	284	1-68
DG	287	1-68
DG	290	1-68
DG	300	1-72
DG	301	1-72
DG	302	1-72
DG	303	1-72
DG	304	1-72
DG	305	1-72
DG	306	1-72
DG	307	1-72
DG	308	1-79
DG	381	1-74
DG	384	1-74
DG	387	1-74
DG	390	1-74
DG	501	1-81
DG	503	1-85
DG	506	1-89
DG	507	1-89
DG	508	1-93
DG	509	1-93
DG	515	1-101
DG	516	1-101
Si	3002	1-106
Si	3705	1-109

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How to Use

This data book contains seven areas of product information. These areas are:

1. Analog Switches
2. Drivers for FET Switches
3. Multi-Channel FET Switches
4. Die Process and Topography Information
5. Burn-In Pin Connections
6. Mechanical Data
7. Appendices

The next pages provide Cross Reference and Selector Guides for rapid determination of the product you desire in your application.

If you have an application and are *not* familiar with the analog switch parameters you need, turn to page 0-8 and choose one of the listed applications which is related. You may select the type of switch recommended and proceed to the data sheets, or, you may select one or more of the important parameters and proceed to the next selector guide.

If you have an application and are familiar with the analog switch parameters you need, turn to page 0-11 to the Product Selector Guide by Parameters or to page 0-12 for the Preferred Product Selector Guide. These guides contain a listing of Siliconix's popular switches with some of their parameters. If you desire a specific switch combination (DPST, Differential Multiplexer) turn to page 0-12 for the Preferred Product Selector Guide. From these guides you will be able to select the device you need. Once you have decided on the analog switch for your application, turn to the data sheet section for more complete electrical specifications of the part; the page number can be found in the Table of Contents.

The Mechanical Data section (Index 6) provides complete dimensional detail (in English and metric rule) for all packages.

For our customers buying chips, Die Topography Information (Index 4) gives complete information by part number for die pad locations for lead bonding.

Complete burn-in specifications and bias conditions are given in Index 5. These are the Siliconix standard burn-in conditions and are encouraged for use by customers doing their own incoming burn-in sampling or for use in their specification drawings.

For more application information, page 7-1 lists Siliconix's current application notes and articles which are available from your local Siliconix sales representative.

To order your analog switches, refer to page 0-21 for Ordering Information and to the last pages for a listing of Siliconix's sales offices world-wide.

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Analog Switch Data Book

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Cross Reference/Substitution Guide
Integrated Circuits

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Direct Replacement: Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications.

Similar Function: Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed, as these parts usually have different pin configurations. Before selecting a device as a substitute, compare the specifications.

Mfgr's Device Number	SILICONIX DEVICE Direct Replacement	Similar Function	Manufacturer's Description
AD7501		DG508	8 × Analog Mux, CMOS
AD7502		DG509	4 × Diff Analog Mux, CMOS
AD7503		DG508	8 × Analog Mux, CMOS
AD7506	DG506		16 × Analog Mux, CMOS
AD7507	DG507		8 × Diff Analog Mux, CMOS
AD7510		DG201	4 × SPST Analog Switch, CMOS
AD7511		DG201	4 × SPST Analog Switch, CMOS
AD7512		DG303	2 × SPDT Analog Switch, CMOS
AD7513	DG200	DG300	2 × SPST Analog Switch, CMOS
AD7516		DG201	4 × SPST Analog Switch, CMOS
AD7519		DG515	4 × SPDT Steering Switch
AH0014		DG303, DG307	DPDT MOS Analog Switch
AH0015		DG172, DG201	4 × SPST MOS Analog Switch
AH0019		DG184, DG302, DG306	2 × DPST MOS Analog Switch
AH0126	DG126		2 × DPST JFET Analog Switch
AH0129	DG129		2 × DPST JFET Analog Switch
AH0133	DG133		2 × DPST JFET Analog Switch
AH0134	DG134		2 × SPST JFET Analog Switch
AH0139	DG139		DPDT Diff JFET Analog Switch
AH0140	DG140		2 × DPST JFET Analog Switch
AH0141	DG141		2 × SPST JFET Analog Switch
AH0142	DG142		2 × DPST JFET Analog Switch
AH0143	DG143		2 × SPST JFET Analog Switch
AH0144	DG144		SPDT Diff JFET Analog Switch
AH0145	DG145		DPDT 2 × Diff JFET Analog Sw
AH0146	DG146		SPDT Diff JFET Analog Switch
AH0151	DG151		2 × SPST JFET Analog Switch
AH0152	DG152		2 × SPST JFET Analog Switch
AH0153	DG153		2 × DPST JFET Analog Switch
AH0154	DG154		2 × DPST JFET Analog Switch
AH0161	DG161		SPDT Diff JFET Analog Switch
AH0162	DG162		SPDT Diff JFET Analog Switch
AH0163	DG163		DPDT Diff JFET Analog Switch
AH0164	DG164		DPDT Diff JFET Analog Switch
AH2114		DG181, 184	DPST JFET Analog Switch
AH5009		DG172	4 × SPST Virtual Gnd Analog Sw
AH5010		DG172	4 × SPST Virtual Gnd Analog Sw
AH5011		DG201	4 × SPST Virtual Gnd Analog Sw
AH5012		DG201	4 × SPST Virtual Gnd Analog Sw
AH5013		DG172(¾)	3 × SPST Virtual Gnd Analog Sw
AH5014		DG172(¾)	3 × SPST Virtual Gnd Analog Sw
AH5015		DG201(¾)	3 × SPST Virtual Gnd Analog Sw
AH5016		DG201(¾)	3 × SPST Virtual Gnd Analog Sw
AM181		DG181	SPST BIFET
AM182		DG182	SPST BIFET
AM184		DG184	2 × DPST BIFET
AM185		DG185	2 × DPST BIFET
AM187		DG187	SPDT BIFET
AM188		DG188	SPDT BIFET
AM190		DG190	2 × SPDT BIFET
AM191		DG191	2 × SPDT BIFET
AM2009		G115, G118	6 × MOS Analog Switch
AM281		DG181	SPST BIFET Switch
AM282		DG182	SPST BIFET Switch
AM3705	SI3705		8 × MOS Analog Mux
AM9709		DG172	4 × SPST Virtual Gnd Analog Sw
AM9710		DG172	4 × SPST Virtual Gnd Analog Sw
AM9711		DG201	4 × SPST Virtual Gnd Analog Sw
AM9712		DG201	4 × SPST Virtual Gnd Analog Sw
AY5-1016		DG507	8 × Diff PMOS Mux (Stgentr)
AY6-4016		DG507	8 × Diff PMOS Mux (Stgentr)
CAG6		DG141(½), DG180(½)	SPST JFET Analog Switch, Very Low r_{DS}
CAG7		DG145, 161, 186, 187	SPDT JFET Analog Switch, Very Low r_{DS}
CAG13		DG181	2 × SPST JFET Analog Switch, Low r_{DS}
CAG14		DG181	SPST JFET Analog Switch, High Speed

Mfgr's Device Number	SILICONIX DEVICE Direct Replacement	Similar Function	Manufacturer's Description
CAG21		DG184	2 × DPST JFET Analog Switch, Low r_{DS}
CAG22		DG181	2 × SPST JFET Analog Switch, Low r_{DS}
CAG23		DG181	2 × SPST JFET Analog Switch, Low r_{DS}
CAG24		DG134	2 × SPST JFET Analog Switch, Low r_{DS} Low Power
CAG27		DG141, DG180	2 × SPST JFET Analog Switch, Very Low r_{DS}
CAG30		DG181(½)	SPST JFET Analog Switch, Low r_{DS}
CAG42		DG181	2 × SPST JFET Analog Switch, Low r_{DS}
CAG45		DG181	2 × SPST JFET Analog Switch, Low r_{DS}
CAG48		DG184	2 × DPST JFET Analog Switch
CD4016		DG201	4 × SPST CMOS Analog Switch
CD4051		DG508	8 Channel CMOS Mux
CD4052		DG509	4 Channel CMOS Diff Mux
CD4067		DG506	16 Channel CMOS Mux
CD4097		DG507	8 Channel CMOS Diff Mux
CDA2		DG181	2 × SPST JFET Analog Switch
CDA18		DG187	SPDT JFET Analog Switch, Fast
CDA23		DG186	SPDT JFET Analog Switch, Fast
CDR5		DG139(½)	Low-Level to High-Level Interface Circuit
CDR125AP	D125AP		6 × FET Driver
CD4052		DG509	4 × Diff CMOS Analog Mux
CD4053		DG170	3 × SPDT CMOS Analog Switch
CD4066		DG201	4 × SPST CMOS Analog Switch
D123	D123		6 × FET Driver
D125	D125		6 × FET Driver
DG111	DGM111		2 × SPST MOS Analog Switch
DG116	DG116		4 × SPST MOS Analog Switch
DG118		DG172	4 × SPST MOS Analog Switch
DG123	DG123		5 × SPST MOS Analog Switch
DG125	DG125		5 × SPST MOS Analog Switch
DG126	DG126		2 × DPST JFET Analog Switch
DG129	DG129		2 × DPST JFET Analog Switch
DG133	DG133		2 × SPST JFET Analog Switch
DG134	DG134		2 × SPST JFET Analog Switch
DG139	DG139		DPDT Diff JFET Analog Switch
DG140	DG140		2 × DPST JFET Analog Switch
DG141	DG141		2 × SPST JFET Analog Switch
DG142	DG142		DPDT Diff JFET Analog Switch
DG143	DG143		SPDT Diff JFET Analog Switch
DG144	DG144		SPDT Diff JFET Analog Switch
DG145	DG145		DPDT Diff JFET Analog Switch
DG146	DG146		SPDT Diff JFET Analog Switch
DG151	DG151		2 × SPST JFET Analog Switch
DG152	DG152		2 × SPST JFET Analog Switch
DG153	DG153		2 × DPST JFET Analog Switch
DG154	DG154		2 × DPST JFET Analog Switch
DG161	DG161		SPDT Diff JFET Analog Switch
DG162	DG162		SPDT Diff JFET Analog Switch
DG163	DG163		DPDT Diff JFET Analog Switch
DG164	DG164		DPDT Diff JFET Analog Switch
DG181	DG181	DG381	2 × SPST JFET Analog Switch
DG181	DG381		2 × SPST JFET Analog Switch
DG182	DG182	DG381	2 × SPST JFET Analog Switch
DG184	DG184	DG384	2 × DPST JFET Analog Switch
DG184	DG384		2 × DPST JFET Analog Switch
DG185	DG185	DG384	2 × DPST JFET Analog Switch
DG187	DG187	DG387	SPDT JFET Analog Switch
DG188	DG188	DG387	SPDT JFET Analog Switch
DG190	DG190	DG390	2 × SPDT JFET Analog Switch
DG190	DG390		2 × SPDT JFET Analog Switch
DG191	DG191	DG390	2 × SPDT JFET Analog Switch

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Cross Reference/Substitution Guide

Integrated Circuits (Cont'd)

Mfgr's Device Number	SILICONIX DEVICE Direct Replacement	Similar Function	Manufacturer's Description
DG200	DG200		2 × SPST CMOS Analog Switch
DG201	DG201		4 × SPST CMOS Analog Switch
DG211	DG211		4 × SPST CMOS Analog Switch
DG300	DG300		2 × SPST CMOS Analog Switch
DG301	DG301		SPDT CMOS Analog Switch
DG302	DG302		2 × DPST CMOS Analog Switch
DG303	DG303		2 × SPDT CMOS Analog Switch
DG304	DG304		2 × SPST CMOS Analog Switch
DG305	DG305		SPDT CMOS Analog Switch
DG306	DG306		2 × DPST CMOS Analog Switch
DG307	DG307		2 × SPDT CMOS Analog Switch
DG308	DG308		4 × SPST CMOS Analog Switch
DG381	DG381		2 × SPST CMOS Analog Switch
DG384	DG384		2 × DPST CMOS Analog Switch
DG387	DG387		SPDT CMOS Analog Switch
DG390	DG390		2 × SPDT CMOS Analog Switch
DG426-DG464	DG126-DG164		See DG126/DG164 preceding for part description
DGM111	DGM111		2 × SPST PMOS Analog Switch
DGM122	DGM122		2 × DPST PMOS Analog Switch
G115	G115		6 × MOS FET Switch
G116	G116		5 × MOS FET Switch
G117	G117		5 × MOS FET Switch
G118	G118		6 × MOS FET Switch
G119	G119		3 × Diff MOS FET Switch
G123	G123		4 × MOS FET Switch
HI-200	DG200		2 × SPST CMOS Analog Switch
HI-201	DG201		4 × SPST CMOS Analog Switch
HI-506	DG506		16 × CMOS Analog Mux
HI-506A	DG506		16 × CMOS Analog Mux
HI-507	DG507		8 × CMOS Diff Analog Mux
HI-507A	DG507		8 × CMOS Diff Analog Mux
HI-508A	DG508		8 × CMOS Analog Mux
HI-509A	DG509		4 × CMOS Diff Analog Mux
HI-1800		DG184, DG302, DG306	2 × DPST CMOS Analog Switch
HI-1800A		DG185, DG302, DG306	2 × DPST CMOS Analog Switch
HI-1818		DG508	8 × CMOS Analog Mux
HI-1818A		DG508	8 × CMOS Analog Mux
HI-1828		DG509	4 × CMOS Diff Analog Mux
HI-1828A		DG509	4 × CMOS Diff Analog Mux
HI-1840		DG506	16 × CMOS Analog Mux
HI-5040		DG182(½), DG200(½), DG300(½), DG304(½)	SPST CMOS Analog Switch
HI-5041		DG182, DG200, DG300, DG304	2 × SPST CMOS Analog Switch
HI-5042		DG188, DG301, DG304	SPDT CMOS Analog Switch
HI-5043	DG191	DG303, DG307, DG390	2 × SPDT CMOS Analog Switch
HI-5044		DG182, DG185(½), DG200, DG300, DG302(½), DG304, DG306(½)	DPST CMOS Analog Switch
HI-5045		DG302, DG306	2 × DPST CMOS Analog Switch
HI-5046		DG191, DG303, DG307	DPDT CMOS Analog Switch
HI-5046A		DG190, DG303 DG307	DPDT CMOS Analog Switch
HI-5047		DG185, DG302, DG306	4PST CMOS Analog Switch
HI5047A		DG184, DG302, DG306	4PST CMOS Analog Switch
HI-5048		DG181, DG300, DG304	2 × SPST CMOS Analog Switch
HI-5049	DG184	DG302, DG306, DG384	2 × DPST CMOS Analog Switch
HI-5050		DG187, DG301, DG305	SPDT CMOS Analog Switch
HI-5051	DG190	DG303, DG307, DG390	2 × SPDT CMOS Analog Switch
HS-1000		DG506	16 × JFET Analog Mux
IH181	DG181		2 × SPST JFET Analog Switch
IH182	DG182		2 × SPST JFET Analog Switch
IH184	DG184		2 × DPST JFET Analog Switch
IH185	DG185		2 × DPST JFET Analog Switch
IH187	DG187		SPDT JFET Analog Switch
IH188	DG188		SPDT JFET Analog Switch
IH190	DG190		2 × SPDT JFET Analog Switch
IH191	DG191		2 × SPDT JFET Analog Switch
IH200		DG200	2 × SPST CMOS Analog Switch
IH201	DG211	DG201	4 × SPST CMOS Analog Switch
IH202		DG201	4 × SPST CMOS Analog Switch
IH5001		DG133(½)	SPST JFET Analog Switch
IH5002		DG134(½)	SPST JFET Analog Switch
IH5003		DG133	2 × SPST JFET Analog Switch

Mfgr's Device Number	SILICONIX DEVICE Direct Replacement	Similar Function	Manufacturer's Description
IH5004		DG134	2 × SPST JFET Analog Switch
IH5005		DG141	2 × SPST JFET Analog Switch
IH5006		DG133	2 × SPST JFET Analog Switch
IH5007		DG134	2 × SPST JFET Analog Switch
IH5009		DG172	4 × SPST Virtual Gnd Analog Sw
IH5010		DG172	4 × SPST Virtual Gnd Analog Sw
IH5011		DG201	4 × SPST Virtual Gnd Analog Sw
IH5012		DG201	4 × SPST Virtual Gnd Analog Sw
IH5013		DG172(¾)	3 × SPST Virtual Gnd Analog Sw
IH5014		DG172(¾)	3 × SPST Virtual Gnd Analog Sw
IH5015		DG201(¾)	3 × SPST Virtual Gnd Analog Sw
IH5016		DG201(¾)	3 × SPST Virtual Gnd Analog Sw
IH5017		DGM111, DG200, DG300, DG304	3 × SPST Virtual Gnd Analog Sw
IH5018		DGM111, DG200, DG300, DG304	2 × SPST Virtual Gnd Analog Sw
IH5019		DGM111, DG200, DG300, DG304	2 × SPST Virtual Gnd Analog Sw
IH5020		DGM111, DG200, DG300, DG304	2 × SPST Virtual Gnd Analog Sw
IH5021		DG200(½), DG300(½), DG304(½)	SPST Virtual Gnd Analog Sw
IH5022		DG200(½), DG300(½), DG304(½)	SPST Virtual Gnd Analog Sw
IH5023		DG200(½), DG300(½), DG304(½)	SPST Virtual Gnd Analog Sw
IH5024		DG200(½), DG300(½), DG304(½)	SPST Virtual Gnd Analog Sw
IH5025		DG172	4 × SPST Positive Signal Analog Switch
IH5026		DG172	4 × SPST Positive Signal Analog Switch
IH5027		DG201	4 × SPST Positive Signal Analog Switch
IH5028		DG201	4 × SPST Positive Signal Analog Switch
IH5029		DG172(¾)	3 × SPST Positive Signal Analog Switch
IH5030		DG172(¾)	3 × SPST Positive Signal Analog Switch
IH5031		DG201(¾)	3 × SPST Positive Signal Analog Switch
IH5032		DG201(¾)	3 × SPST Positive Signal Analog Switch
IH5033		DGM111, DG200, DG300, DG304	2 × SPST Positive Signal Analog Switch
IH5034		DGM111, DG200, DG300, DG304	2 × SPST Positive Signal Analog Switch
IH5035		DGM111, DG200, DG300, DG304	2 × SPST Positive Signal Analog Switch
IH5036		DGM111, DG200, DG300, DG304	2 × SPST Positive Signal Analog Switch
IH5037		DG200(½), DG300(½), DG304(½)	SPST Positive Signal Analog Switch
IH5038		DG200(½), DG300(½), DG304(½)	SPST Positive Signal Analog Switch
IH5040		DG182(½), DG200(½), DG300(½), DG304(½)	SPST CMOS Analog Switch
IH5041		DG182, DG200, DG300, DG304	2 × SPST CMOS Analog Switch
IH5042		DG188, DG301, DG305	SPDT CMOS Analog Switch
IH5043	DG191	DG303, DG307, DG390	2 × SPST CMOS Analog Switch
IH5044		DG182, DG185(½), DG200, DG300, DG302(½), DG304, DG306(½)	DPST CMOS Analog Switch
IH5045	DG185	DG302, DG306, DG384	2 × DPST CMOS Analog Switch
IH5046		DG191, DG303, DG407	DPDT CMOS Analog Switch
IH5047		DG185, DG302, DG306	4PST CMOS Analog Switch
IH5048		DG181, DG300, DG304	2 × SPST CMOS Analog Switch
IH5049	DG184	DG302, DG306 DG384	2 × DPST CMOS Analog Switch
IH5050		DG187, DG301, DG305	SPDT CMOS Analog Switch
IH5051	DG190	DG303, DG307 DG390	2 × SPDT CMOS Analog Switch

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Cross Reference/Substitution Guide

Integrated Circuits (Cont'd)

Mfgr's Device Number	SILICONIX DEVICE Direct Replacement	Similar Function	Manufacturer's Description
IH5052	DG211	DG201	4 × SPST CMOS Analog Switch
IH5053		DG211	4 × SPST CMOS Analog Switch
IH5060	DG506		16 × CMOS Analog Mux
IH5070	DG507		8 × Diff CMOS Analog Mux
IH6108	DG508		8 × CMOS Analog Mux
IH6116	DG506		16 × CMOS Analog Mux
IH6208	DG509		4 × Diff CMOS Analog Mux
IH6216	DG507		8 × Diff CMOS Analog Mux
LFXX331		DG201	4 × SPST JFET Analog Switch
LFXX332		DG201	4 × SPST JFET Analog Switch
LFXX333		DG201	4 × SPST JFET Analog Switch
LFXX201	DG201		4 × SPST JFET Analog Switch
LFXX202		DG201	4 × SPST JFET Analog Switch
LFXX506		DG506	16 × CMOS Analog Mux
LFXX507		DG507	8 × Diff CMOS Analog Mux
LFXX508	DG508		8 × CMOS Analog Mux
LFXX509	DG509		4 × Diff CMOS Analog Mux
MM4504		G115, G118	6 × MOS Analog Switch
MM5504		G115, G118	6 × MOS Analog Switch
MPC-16S	DG506		16 × CMOS Analog Mux
MPC-8D	DG507		8 × Diff CMOS Analog Mux
MPC-8S	DG508		8 × CMOS Analog Mux
MPC-4D	DG509		4 × Diff CMOS Analog Mux
MPM-8S	DG508		8 × MOS Analog Mux
MC1150L		DG501	8 × MOS Analog Mux
MC1151L		DG511	4 × Diff MOS Analog Mux
MC14016		DG172, 201	4 × SPST CMOS Analog Switch
MC14051		DG508	8 × CMOS Analog Mux
MC14052		DG509	4 × Diff CMOS Analog Mux
MC14053		DG170	3 × SPDT CMOS Analog Switch
MC14066		DG172, 201	4 × SPDT CMOS Analog Switch
MC14529		DG508, 509	8 × CMOS Analog Mux
MMD-8		DG507	8 × Diff CMOS Analog Mux
MM16		DG506	16 × CMOS Analog Mux

Mfgr's Device Number	SILICONIX DEVICE Direct Replacement	Similar Function	Manufacturer's Description
MM4504		G118	6 × PMOS Analog Mux
MM5504		G118	6 × PMOS Analog Mux
MP7510		DG201	4 × SPST CMOS Analog Switch
MP7511		DG201	4 × SPST CMOS Analog Switch
MP7513		DG200, DG300	2 × SPST CMOS Analog Switch
MP7516		DG506	16 × CMOS Analog Mux
MUX08	DG508		8 × CMOS Analog Mux
MUX16	DG506		16 × CMOS Analog Mux
MUX24	DG509		4 × Diff CMOS Analog Mux
MUX28	DG507		8 × Diff CMOS Analog Mux
MUX88			8 × Diff JFET Analog Mux
MVD409		DG507	4 × Diff CMOS Analog Mux
MVD807		DG507	8 × Diff CMOS Analog Mux
MV808		DG508	8 × Diff CMOS Mux
MXD409		DG509	4 × Diff CMOS Analog Mux
MXD807		DG507	8 × Diff CMOS Analog Mux
MX1606		DG506	16 × CMOS Analog Mux
37052		DG501	8 × Analog Mux, MOS
37053	SI3705	DG501	8 × Analog Mux, MOS
37082	SI3705	DG501	8 × Analog Mux, MOS
37083	SI3705	DG501	8 × Analog Mux, MOS
TL182	DG182	DG381	SPST BIFET
TL185	DG185	DG384	2 × DPST BIFET
TL188	DG188	DG387	SPDT BIFET
TL190	DG190	DG390	2 × SPDT BIFET
TL191	DG191	DG390	2 × SPDT BIFET
TL601		DG301	SPDT PMOS Analog Switch
TL604		DG301	SPDT PMOS Analog Switch
TL607		DG301	SPDT PMOS Analog Switch
UC4250		L144(1/3)	Low Power Op Amp
UC4252		L144(2/3)	2 × Low Power Op Amp
UC4253		L144	Triple Low Power Op Amp

TEMPERATURE RANGE AND PACKAGE CROSS REFERENCE

The following table relates Siliconix packages and temperatures to those of several competitors. The chart is further illustrated by including examples in the table.

This table and the accompanying IC Cross Reference are intended to be used with intelligent study of the applicable data sheets and not as a guaranteed replacement guide.

Company	Temperature Range			Package					Examples			
									DG200	DG201	DG181	DG506
	– 55–125°C	– 20–85°C	– 0–70°C	Hermetic Dip	Hermetic Dip	Hermetic F.P.	Hermetic Metal Can	Plastic	2XSPST CMOS	4XSPST CMOS	2XSPST JFET	16X MUX CMOS
Siliconix	A	B	C	P	K	L	A	J	DG200AA DG200CJ	D6201AP DG201CJ	DG181AA DG181BP	DG506AR DG506CJ
Harris	2	4 9	5	1	1	9	2	3	HI200-2 HI5041-5 HI5048-2	HI201-2		HI506-2 HI1840
Intersil	M	I	C	D P	J	F L	T A	P	IH5041M IH5048C IH200C	IH201M IH202I IH5052C IH5053C	IH5005 IH5006	IH6116C
Analog Devices	A B C	J K L	S T U						AD7513S	AD7510DIJ AD7516J		AD7506S
National	M 1	C 2	3	J D	J D	F W	H	N		LF11201 CD4066BC CD4016C AM193	AMIBI	LF1106
PMI				Y Q X	Q X X	M	K	X Q Y		SSS7510A SSS7511A		MUX16A
TI	M	C	L	JA JB JP	JA JB JP	T FA J	L LA	N P		TP4016A/B	TL182M	

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Product Selector Guide by Applications

Application	Feature of Application	Important Switch Parameters	Major Tradeoffs	Suggested Switches
Battery Operated or Battery Back-Up Supply	1) Low Power	Low Supply Current		**CMOS DG304-DG308** DG300-DG303, DG381-DG390 JFET DG126-DG164
	2) Minimum Number of Power Supplies	Only One or Two Supplies Needed		**CMOS DG300-DG308** (Can Also Be Used As Single Supply) CMOS DG200, DG201 (For MUX: DG506-DG509)
	3) Low Standby Power	Low Standby Current		**CMOS DG304-DG308** JFET DG126-DG164
Audio	1) Low Signal Distortion	Low $r_{ds(on)}$ Constant $r_{ds(on)}$	JFET is Constant, $r_{ds(on)}$ Signal Range Limited Toward Negative Supply CMOS Slight $r_{ds(on)}$ Variation, Full Signal Range	**JFET DG180-DG191** CMOS DG300-DG308, DG381-DG390
	2) Low Noise	Low $r_{ds(on)}$		CMOS DG300-DG308, DG381-DG390 JFET DG180-DG191
	3) Wide Signal Range	±15 V Signal Range		**CMOS DG300-DG308,** DG381-DG390 CMOS DG200, DG201 (MUX: DG506-DG509)
		Signal Range is From the Positive Supply to Above the Negative Supply	Higher $r_{ds(on)}$ (Must Stay Above Negative Supply By 5 V to 7.5 V)	**JFET (75Ω) DG182, DG185, DG188, DG191** (10 Ω, 30 Ω) Remainder of DG181-DG190 Family
	4) Large Dynamic Range	Wide Signal Range and Low Thermocouple Noise		**CMOS DG304-DG308** DG300-DG303, DG381-DG390
Video (High Frequency)	1) High OFF Impedance, Small Feedthrough of Signal	High OFF Isolation	Higher $r_{ds(on)}$	**JFET (30 Ω, 75 Ω) DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191** CMOS DG200, DG201 CMOS DG300-DG308, DG381-DG390
	2) Good Impedance Matching, Minimum Signal Drop Across Switch	Low $r_{ds(on)}$	Lower OFF Isolation	**JFET (10 Ω) DG180, DG183, DG186, DG189** (30 Ω) DG181, DG184, DG187, DG190 CMOS DG300-DG308

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Product Selector Guide by Applications

Application	Feature of Application	Important Switch Parameters	Major Tradeoffs	Suggested Switches
Differential Signal Switching	1) Good Matching of Switch Parameters	Monolithic Switch		**CMOS DG300, DG302, DG303, DG304, DG306, DG307, DG381, DG384, DG390** CMOS DG200, DG201
	2) Low Thermocouple Offset Voltage	Drain and Source of FET Switch in Close Proximity on *Small Chip*	JFET Switches Not Monolithic	**JFET DG183, DG184, DG185**
		Low Power Dissipation on Switch Driver		**CMOS DG304, DG306, DG307, DG308** DG300-DG303 DG381-DG390
Small Signal (<1 V)	1) Low Noise	Low $r_{ds(on)}$	Higher Leakages	**JFET (10 Ω) DG180, DG183, DG186, DG189** (30 Ω, 75 Ω) (Remainder of DG181-DG191 Family) CMOS DG300-DG307, DG381-DG390
	2) High Impedance Inputs or Load	Low Leakage	Higher $r_{ds(on)}$	**CMOS DG300-DG307, DG381-DG390, DG200-DG201** JFET DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191
	3) Low Thermocouple Offset Voltage	Low Power Switch		**CMOS DG304-DG307** DG300-DG303, DG381-DG390
		Drain and Source of FET Switch in Close Proximity on *Small Chip*		JFET DG180-DG190
Multiplexing	1) Break-Before-Make Switching	t_{on} is Greater Than t_{off}		**CMOS DG506, DG507, DG508, DG509** PMOS DG501, DG503
	2) Binary Controlled Logic Inputs	Binary Decoding Stage on Chip		
	3) Differential Multiplexing	Dual Switching Action		CMOS DG507, DG509
	4) D/A Conversion	Binary Weighted ON Resistance and Channel Resistance to Minimize Error		NMOS DG515, DG516

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Product Selector Guide by Applications

Application	Feature of Application	Important Switch Parameters	Major Tradeoffs	Suggested Switches
Sample and Hold	1) Low Droop Rate	Low Leakage	Higher ON Resistance	**CMOS DG300-DG308, DG381-DG390** JFET DG180-DG191 CMOS DG200, DG201
	2) Low Sample to Hold Offset	Low Charge Coupling	Higher ON Resistance	**CMOS DG200, DG201** CMOS DG300-DG308 JFET DG181, DG182 (30 Ω, 75 Ω) DG184, DG185, DG187, DG188, DG190, DG191
	3) Fast Acquisition Speed	Low ON Resistance	Higher Leakage Higher Charge Coupling	**JFET (10 Ω) DG180, DG183, DG186, DG189** (30 Ω, 75 Ω) Remainder of DG181-DG191 Family CMOS DG300-DG307, DG381-DG390 CMOS DG200, DG201
Switching to High Impedance Inputs	1) Low Error Voltage	Low Leakage		**CMOS DG300-DG307, DG381-DG390** **DG200-DG201** JFET DG180-DG191
	2) Low Switching Transient Error Voltage	Low Charge Coupling		**CMOS DG200, DG201** DG300-DG307, DG381-DG390
Low Cost	1) Best Performance for Lowest Cost	Monolithic Good Switch Performance		**CMOS DG211, DG300-DG308** DG200, DG201, DG381-DG390
Military System	1) Hi-Rel Specified			**JM38510/XXXXX** (See Current Certified QPL or BS9000 Listings)

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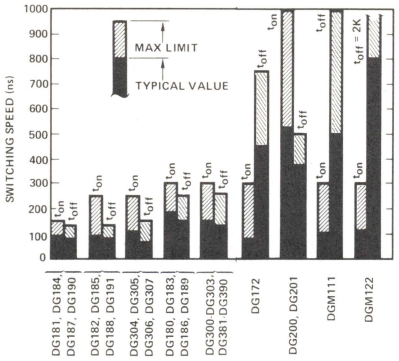
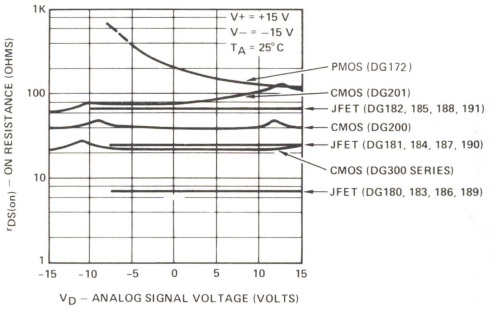
Product Selector Guide by Parameters

TYPICAL PERFORMANCE CHARACTERISTICS

Typical t_{on}/t_{off}



Typical $r_{DS(on)}$ vs V_D



NOTE: The CMOS switches are the only ones capable of switching signals down to the negative supply.

SELECTION GUIDE, LISTED BY PERFORMANCE:

$r_{DS(on)}$	
Device No.	(Ω)
DG180, DG183 DG186, DG189	10 Ω
DG181, DG184, DG187, DG190	30 Ω
DG300-DG303 DG304-DG307 DG381-DG390	50 Ω
DG200	70 Ω
DG182, DG185, DG188, DG191	75 Ω
DGM111	75 to 200 Ω
DG201	175 Ω
DG501*	150 to 250 Ω
DG172, DG173	150 to 450 Ω
DG506*, DG507* DG508*, DG509*	400 Ω
DG503*	150 to 800 Ω
DG170	200 to 800 Ω

t_{ON}/t_{OFF}	
Device No.	(ns)
DG181, DG184, DG187, DG190	150/ 130
DG182, DG185, DG188, DG191	250/ 130
DG304, DG305, DG306, DG307	250/ 150
DG180, DG183, DG186, DG189	300/ 250
DG300-DG303 DG381-DG390	300/ 250
DG172	300/ 750
DG200, DG201	1000/ 500
DGM111	300/1000
DGM122	300/2000

Analog Signal Range (with ±15 V supply)	
Device No.	(Volts)
DG200, DG201, DG506*, DG507* DG508*, DG509*	+15 to –15 V
DG300-DG303 DG304-DG307 DG381-DG390	+15 to –15 V
DG182, DG185, DG188, DG191	+15 to –10 V
DG180, DG181, DG183, DG184, DG186, DG187, DG189, DG190	+15 to –7.5 V
DG170, DG172, DG173, DGM111, DGM122	+15 to –5 V

*Multiplexers

Better performance than shown can be obtained from Siliconix analog switches by special sorting at customer request, or by using discrete FET devices chosen for optimal switching characteristics.

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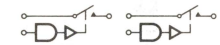
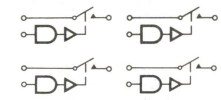
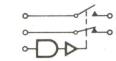
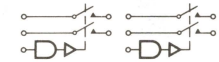
Preferred Product Selector Guide

ANALOG SWITCHES

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec) t_{ON}	Switching Time (μsec) t_{OFF}	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. $V+$	(−) Sup. $V-$	Logic Sup. V_L	Ref. Sup. V_R	Comments	Switch Configuration
TWO CHANNEL SPST														
DGM111	PMOS	+10 to −10	75-200	1	0.3	1.0	0.5	4.6	10	−20	5	–		
DG180	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+15 to − 7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG181	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	**2 SPST Switches per Package**
		+15 to − 7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG182	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG200	CMOS	+15 to −15	70	2	1.0	0.5	0.8	2.4	15	−15	–	(Note 3)		
DG300	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In	
DG304	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In	
DG381	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG181 Pin Out	
FOUR CHANNEL SPST														
DG201	CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	–	(Note 3)		
DG211	CMOS	+15 to −15	175	2	0.5	0.4	0.8	2.4	15	−15	–	5	Low Cost, TTL In	**4 SPST Switches per Package**
DG308	CMOS	+15 to −15	100	1	0.17	0.095	3.5	11.0	15	−15	–	–	Low Cost, CMOS In	
ONE CHANNEL SPDT														
DG186	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to − 7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG187	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	**1 SPDT Switch per Package**
	N-JFET	+15 to − 7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG188	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG301	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In	
DG305	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In	
DG387	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG187 Pin Out	
TWO CHANNEL SPDT														
DG189	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to − 7.5	10	10	0.3	0.25	0.8	2.0	15	15	5	0	15 V Supplies	
DG190	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	20	5	0	Break-Before-Make	**2 SPDT Switches per Package**
	N-JFET	+15 to − 7.5	30	1	0.15	0.13	0.8	2.0	15	15	5	0	15 V Supplies	
DG191	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	20	5	0	Break-Before-Make	
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	15	5	0	15 V Supplies	
DG303	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	15	–	–	Low Power TTL In	
DG307	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	15	–	–	Low Power, CMOS In	
DG390	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	15	–	–	Low Power, DG190 Pin Out	
TWO CHANNEL DPST														
DGM122	PMOS	+10 to −10	100-450	3	0.3	2.0	0.4	1 mA (1)	10	20	5	0		
DG183	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	20	5	0	Break-Before-Make	
	N-JFET	+15 to − 7.5	10	10	0.3	0.25	0.8	2.0	15	15	5	0	15 V Supplies	
DG184	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	20	5	0	Break-Before-Make	**2 DPST Switches per Package**
	N-JFET	+15 to − 7.5	30	1	0.15	0.13	0.8	2.0	15	15	5	0	15 V Supplies	
DG185	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	20	5	0	Break-Before-Make	
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	15	5	0	15 V Supplies	
DG302	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	15	–	–	Low Power, TTL In	
DG306	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	15	–	–	Low Power, CMOS In	
DG384	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	15	–	–	Low Power, DG184 Pin Out	

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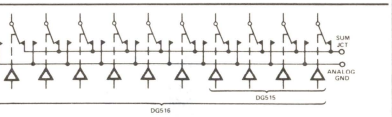
Preferred Product Selector Guide (Cont'd)

ANALOG SWITCHES (Continued)

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec) t_{ON}	Switching Time (μsec) t_{OFF}	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. V+	Opt. Supply Voltage (V) (−) Sup. V−	Opt. Supply Voltage (V) Logic Sup. V_L	Opt. Supply Voltage (V) Ref. Sup. V_R	Comments
FOUR CHANNEL SPDT D/A CONVERTER SUMMING NODE SWITCHES													
DG515	NMOS	(see comments)	40	0.12	0.17	0.5	7.5	8.0	0	–	–	R_1 = 6.25 Ω, R_2 = 12.5 Ω, R_3 = 25 Ω, R_4 = 50 Ω
TEN CHANNEL SPDT D/A CONVERTER SUMMING NODE SWITCHES													
DG516	NMOS	(see comments)	40	0.12	0.17	0.5	7.5	8.0	0	–	–	–	R_1 = 100 Ω, R_2 = 200 Ω, R_3 = 400 Ω, R_4 = 800 Ω, R_5 = 1600 Ω, R_6 = 10 = 3200 Ω

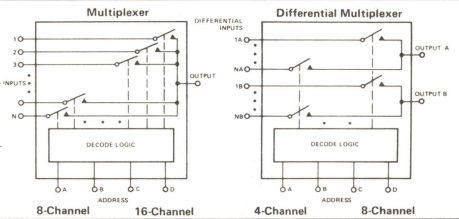
Switch Configuration



ANALOG MULTIPLEXERS

Basic Part No.	Process Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$	Transition Time (μsec) (Note 2)	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. V+	Opt. Supply Voltage (V) (−) Sup. V−	Opt. Supply Voltage (V) Ref. Sup. V_R	Comments
EIGHT CHANNEL MUX + ENABLE											
DG501	PMOS	+ 5 to − 5	150-250	8	1.5	0.6	3.5	5	−20	0	Logic Pullup Resistors
DG503	PMOS	+10 to −10	150-800	8	1.5	0.6	8.5	10	−20	0	
DG508	CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	–	Break-Before-Make
SIXTEEN CHANNEL MUX + ENABLE											
DG506	CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	(Note 3)	Break-Before-Make
FOUR CHANNEL DIFFERENTIAL MUX + ENABLE											
DG509	CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	–	Break-Before-Make
EIGHT CHANNEL DIFFERENTIAL MUX + ENABLE											
DG507	CMOS	+15 to −15	400	5	1.0	0.8	2.4	15	−15	(Note 3)	Break-Before-Make

Switch Configuration



DRIVERS FOR FET SWITCHES

Basic Part No.	Inputs	Outputs	Function and Uses	ON Level $V_{(out)}$ ON to V− At Rated Current(s)	OFF Level $V_{(out)}$ OFF At Rated Current Or $I_{(out)}$ OFF At Rated Voltage	Input Logic for V_{OUT} (low)	Input Limits V_{INL} (V)	Input Limits V_{INH} (V) (I_{INH}) (mA)	Optimum Supply Voltages (V) V+	V−	V_L	V_R	Switching Time (μs) t_{ON}	Switching Time (μs) t_{OFF}
D125	6	6	Six Separate MOSFET-Drivers	0.4 V @ 5 mA	0.1 μA @ 10 V	0	0.5	4.6	(Note 5)	−20	5	–	0.6	1.2
D129	7	4	Four Channel (BV = 50) MOSFET-Driver with Decode	0.7 V @ 10 mA	0.1 μA @ 10 V	1	0.7	2.2	(Note 5)	20	–	–	0.25	0.8
D139	2	4	Dual High-Speed Drivers/with Complimentary Outputs	1.1 V @ 10 μA 1.5 V @ 2 mA	V_1 − 2 V @ 2 mA	Output and Compliment Available	0.8 0.8	2.0 2.0	10 10	20 20	5 5	0 0	0.17 0.17	0.2 0.2

MULTIPLE FET SWITCHES

Basic Part No.	Sources	Drains	Gates	Switch Function	Switch Type	r_{DS} MAX (Ω) @V_S = +10 V	r_{DS} MAX (Ω) @V_S = −10 V	BV_{DSS}	$I_{S(off)}$ (nA)	$V_{GS(th)}$ Min	$V_{GS(th)}$ Max	
G115	6	1	6	SP6T	PMOS	100	450	−30	0.5	−1.5	−4.0	6 Switches, Common Out
G123	4	2	4	2XSPDT	PMOS	100	450	−30	0.5	−1.5	−4.0	4 Switches

NOTES:
1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. V_{REF} = 1.5 V is used when supply voltages < ± 15 V are used. Not needed when supply voltages of ± 15 V are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to + 10 V.

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Process Option Flow Chart

The Process Option Flow Chart shows the standard screening options provided by Siliconix for Analog Switches

Column 1: Denotes the screening process for MIL-883, Class B. To order a part screened to this option, add a "/883" following the package suffix letter. If Group B or C Quality Conformance is also required, call out as a separate line item. Parts in this classification are carried in inventory.

Column 2: Is the screening procedure for military grade standard products ("A" temperature suffix).

Column 3: Is the normal screening procedure for industrial and commercial grade products (B and C temperature suffixes). An industrial and commercial grade product (B and C temperature range) may be given a 160 hour burn-in at 125°C by adding a Dash 4 (–4) following the package suffix letter.

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Process Option Flow Chart

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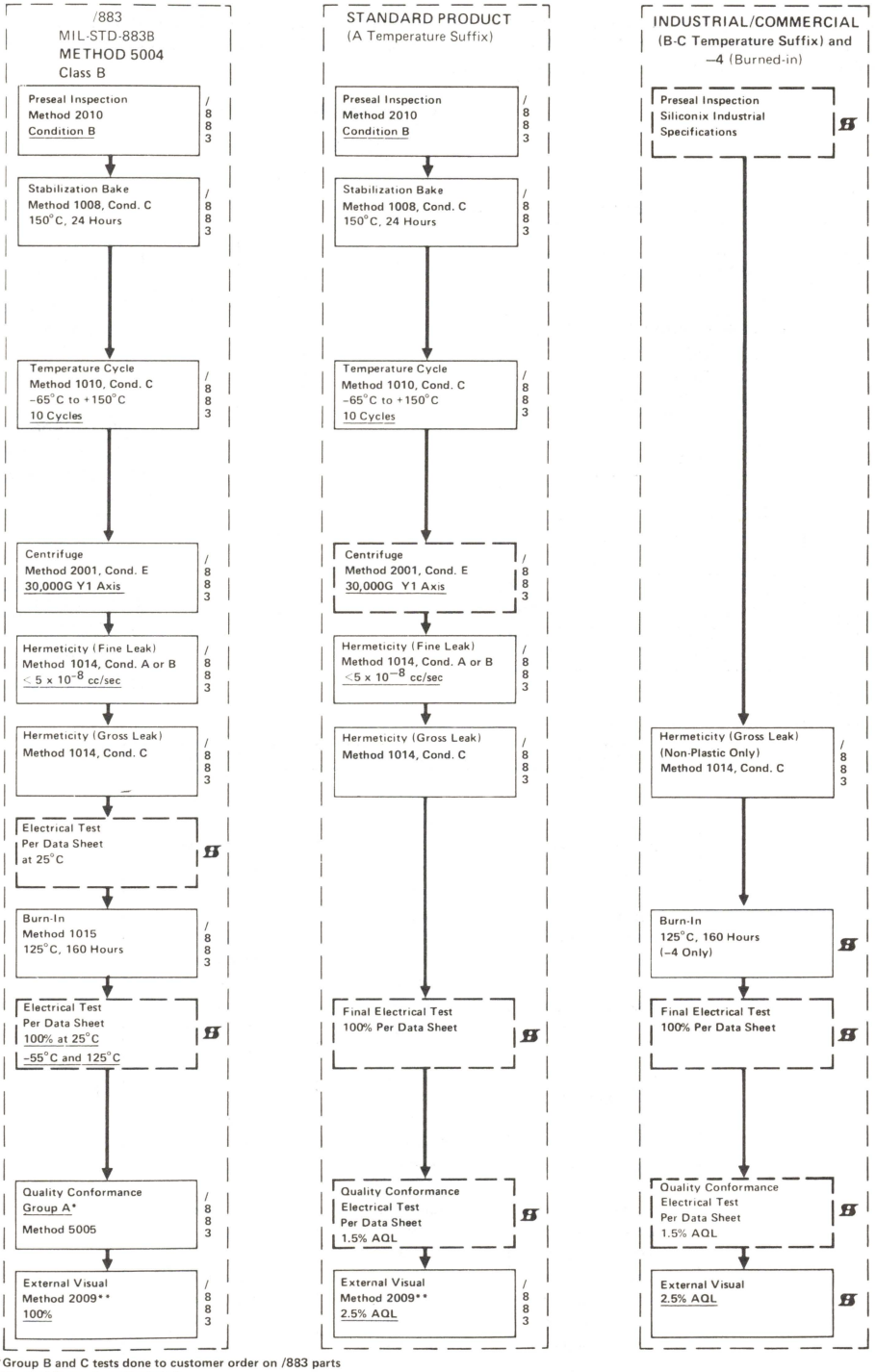

*Group B and C tests done to customer order on /883 parts
**Physical Dimensions Excluded
The latest revision of MIL-STD-883 is applicable

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JAN 38510 Analog Switches

Siliconix

"Several Siliconix Analog Switches are available fully certified on the QPL (Qualified Parts List) published monthly by Defense Electronics Supply Center (DESC). The QPL numbers follow this format JM38510/XXXXX. Refer to the current Siliconix Price List for available part types and order numbers."

JAN Part Numbering System

J M38510 /111 07 B E C

"JAN" Certification Mark

Military Designator

Detail Specification (Slash Sheet)

/111 — DG181 Series
/116 — DG300 Series
/123 — DG200 Series

Device Type

/111	01 — DG181	05 — DG187
	02 — DG182	06 — DG188
	03 — DG184	07 — DG190
	04 — DG185	08 — DG191
/116	01 — DG300	05 — DG304
	02 — DG301	06 — DG305
	03 — DG302	07 — DG306
	04 — DG303	08 — DG307
/123	03 — DG200	
	04 — DG201	

Lead Finish

A — Solder dip
B — Bright tin plate
C — Gold plate

Case Outline

C — 14 Lead side braze
E — 16 Lead side braze
I — 10 Lead can

Device Class

S — Class S
B — Class B
C — Class C

Part Number	Order Part Number	Generic Part Number
JM38510/11101BCC	SJM181BCC	DG181AP/883
JM38510/11101BIC	SJM181BIC	DG181AA/883
JM38510/11102BCC	SJM182BCC	DG182AP/883
JM38510/11102BIC	SJM182BIC	DG182AA/883
JM38510/11103BEC	SJM184BEC	DG184AP/883
JM38510/11104BEC	SJM185BEC	DG185AP/883
JM38510/11105BCC	SJM187BCC	DG187AP/883
JM38510/11105BIC	SJM187BIC	DG187AA/883
JM38510/11106BCC	SJM188BCC	DG188AP/883
JM38510/11106BIC	SJM188BIC	DG188AA/883
JM38510/11107BEC	SJM190BEC	DG190AP/883
JM38510/11108BEC	SJM191BEC	DG191AP/883
JM38510/11601BCC	SJM300BCC	DG300AP/883
JM38510/11601BIC	SJM300BIC	DG300AA/883
JM38510/11602BCC	SJM301BCC	DG301AP/883
JM38510/11602BIC	SJM301BIC	DG301AA/883
JM38510/11603BCC	SJM302BCC	DG302AP/883
JM38510/11604BCC	SJM303BCC	DG303AP/883
JM38510/11605BCC	SJM304BCC	DG304AP/883
JM38510/11605BIC	SJM304BIC	DG304AA/883
JM38510/11606BCC	SJM305BCC	DG305AP/883
JM38510/11606BIC	SJM305BIC	DG305AA/883
JM38510/11607BCC	SJM306BCC	DG306AP/883
JM38510/11608BCC	SJM307BCC	DG307AP/883
JM38510/12303BCC	SJM200BCC	DG200AP/883
JM38510/12303BIC	SJM200BIC	DG200AA/883
JM38510/12304BEC	SJM201BEC	DG201AP/883

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JM38510/883 Process Option Flow Chart

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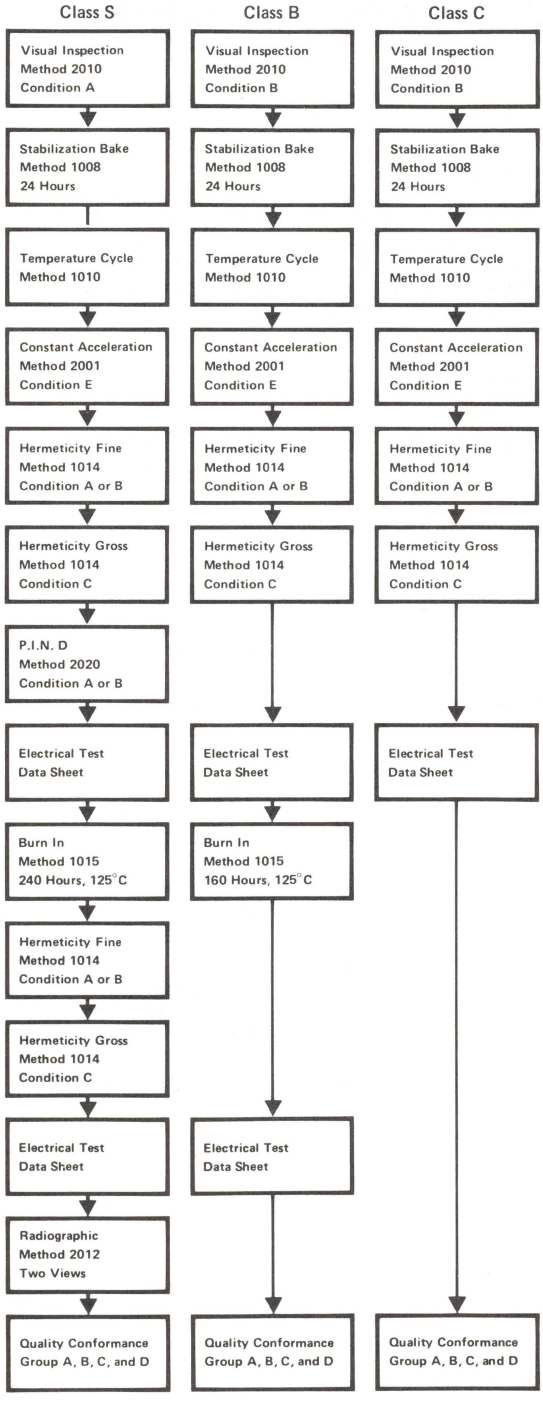

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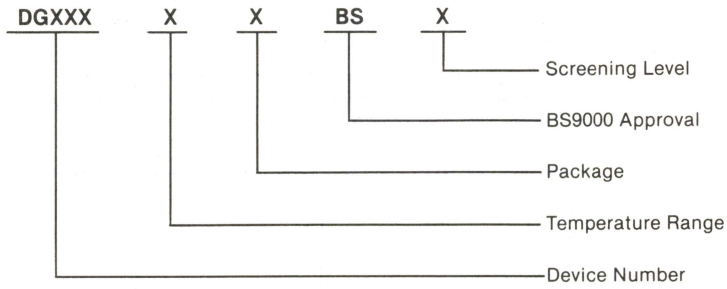
BS9000 Approved Analog Switches

Siliconix is the first company to receive BS9000 approval for analog switch devices. The advantages of such approval are:

- a controlled inspection procedure is known to the customer, so reduces the customer's need for Goods Inwards Inspection
- a more consistent quality of product
- easier interchangeability of suppliers
- a product of known quality levels with, in general, a minimal increase in costs

It is the policy of the UK government to encourage the growth of the BS9000 scheme for the benefit of both government and industry. The Ministry of Defense is therefore insisting on the maximum possible use of BS9000 components in defense equipment. Intending suppliers will be expected to ensure that their components have been specified and received Qualification Approval with the BS9000 scheme.

Interpretation of Ordering Information



Key

Temperature Range

A	– 55°C to 125°C
B	– 20°C to 85°C

Package

A	Metal Can
L	Flatpack
P	Dual-In-Line

Screening Level

(Blank)	Full Assessment
S1	Screening Level S1
S2	Screening Level S2
S3	Screening Level S3
S4	Screening Level S4

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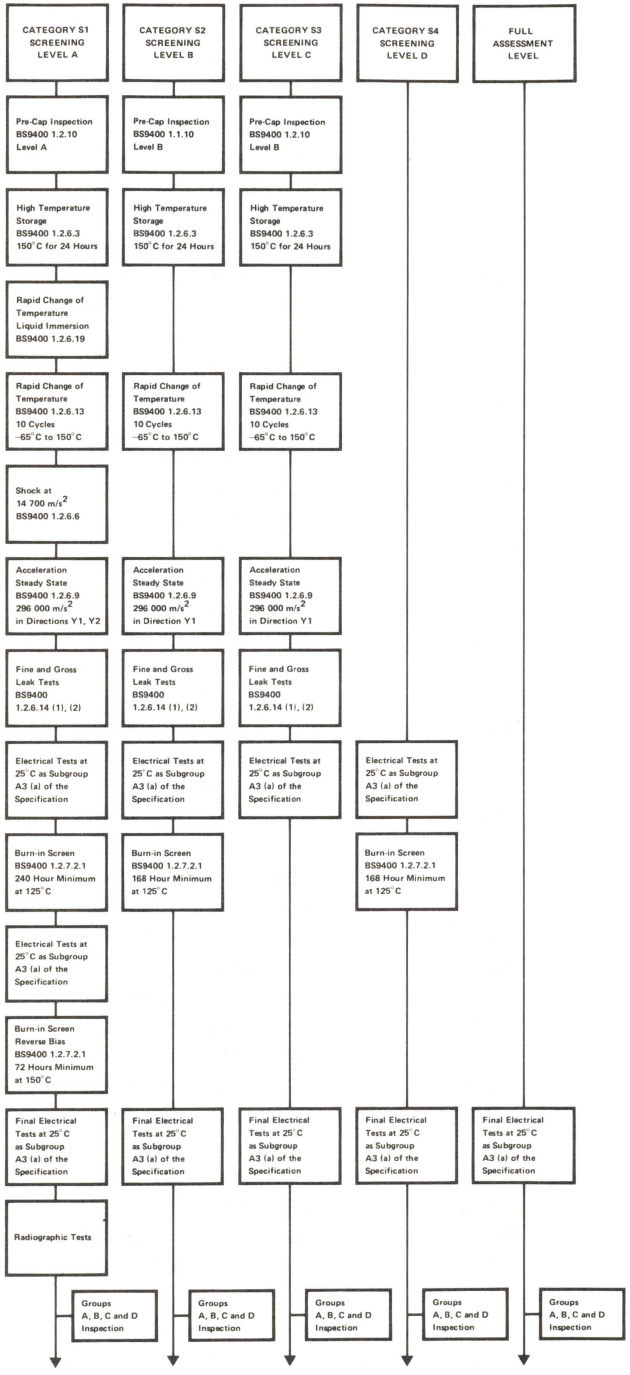
BS9000 Series Process Option Flow Chart

Siliconix


CATEGORY S1 SCREENING LEVEL A
CATEGORY S2 SCREENING LEVEL B
CATEGORY S3 SCREENING LEVEL C
CATEGORY S4 SCREENING LEVEL D
FULL ASSESSMENT LEVEL
Pre-Cap Inspection BS9400 1.2.10 Level A
Pre-Cap Inspection BS9400 1.1.10 Level B
Pre-Cap Inspection BS9400 1.2.10 Level B
High Temperature Storage BS9400 1.2.6.3 150°C for 24 Hours
High Temperature Storage BS9400 1.2.6.3 150°C for 24 Hours
High Temperature Storage BS9400 1.2.6.3 150°C for 24 Hours
Rapid Change of Temperature Liquid Immersion BS9400 1.2.6.19
Rapid Change of Temperature BS9400 1.2.6.13 10 Cycles −65°C to 150°C
Rapid Change of Temperature BS9400 1.2.6.13 10 Cycles −65°C to 150°C
Rapid Change of Temperature BS9400 1.2.6.13 10 Cycles −65°C to 150°C
Shock at 14 700 m/s^2 BS9400 1.2.6.6
Acceleration Steady State BS9400 1.2.6.9 296 000 m/s^2 in Directions Y1, Y2
Acceleration Steady State BS9400 1.2.6.9 296 000 m/s^2 in Direction Y1
Acceleration Steady State BS9400 1.2.6.9 296 000 m/s^2 in Direction Y1
Fine and Gross Leak Tests BS9400 1.2.6.14 (1), (2)
Fine and Gross Leak Tests BS9400 1.2.6.14 (1), (2)
Fine and Gross Leak Tests BS9400 1.2.6.14 (1), (2)
Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Burn-in Screen BS9400 1.2.7.2.1 240 Hour Minimum at 125°C
Burn-in Screen BS9400 1.2.7.2.1 168 Hour Minimum at 125°C
Burn-in Screen BS9400 1.2.7.2.1 168 Hour Minimum at 125°C
Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Burn-in Screen Reverse Bias BS9400 1.2.7.2.1 72 Hours Minimum at 150°C
Final Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Final Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Final Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Final Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Final Electrical Tests at 25°C as Subgroup A3 (a) of the Specification
Radiographic Tests
Groups A, B, C and D Inspection
Groups A, B, C and D Inspection
Groups A, B, C and D Inspection
Groups A, B, C and D Inspection
Groups A, B, C and D Inspection

INSPECTION REQUIREMENTS All tests to be conducted at T_{amb} = 25°C unless otherwise specified. Samples submitted to tests marked 'D' shall not be accepted for release under BS9000 (see 2.6.5 of BS9000 Part 1).
Flow chart for 100% screening test procedures (see also Inspection Requirements) Production batches containing greater than 10% defective units subsequent to Burn-in will not be issued for release.
Radiographic tests Each device shall be examined, for extraneous matter and assembly defects, in the X and Y directions.

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BS9000 Approved Parts

Siliconix

DEVICE PART NUMBER	BS DETAIL SPECIFICATION
DG126	9491-F-0814 to 9491-F-0831
DG129	9491-F-0832 to 9491-F-0849
DG133	9491-F-0850 to 9491-F-0867
DG134	9491-F-0868 to 9491-F-0885
DG139	9491-F-0886 to 9491-F-0903
DG140	9491-F-1030 to 9491-F-1038
DG141	9491-F-1039 to 9491-F-1056
DG142	9491-F-0904 to 9491-F-0921
DG143	9491-F-0922 to 9491-F-0939
DG144	9491-F-0940 to 9491-F-0957
DG145	9491-F-1084 to 9491-F-1092
DG146	9491-F-1093 to 9491-F-1110
DG151	9491-F-1057 to 9491-F-1074
DG152	9491-F-0958 to 9491-F-0975
DG153	9491-F-1075 to 9491-F-1083
DG154	9491-F-0976 to 9491-F-0993
DG161	9491-F-1111 to 9491-F-1128
DG162	9491-F-0994 to 9491-F-1011
DG163	9491-F-1129 to 9491-F-1137
DG164	9491-F-1012 to 9491-F-1029
DG180	9491-F-0688 to 9491-F-0714
DG181	9491-F-0508 to 9491-F-0534
DG182	9491-F-0535 to 9491-F-0561
DG183	9491-F-0733 to 9491-F-0750
DG184	9491-F-0562 to 9491-F-0579
DG185	9491-F-0580 to 9491-F-0597
DG186	9491-F-0751 to 9491-F-0777
DG187	9491-F-0598 to 9491-F-0624
DG188	9491-F-0625 to 9491-F-0651
DG189	9491-F-0715 to 9491-F-0732
DG190	9491-F-0652 to 9491-F-0669
DG191	9491-F-0670 to 9491-F-0687
DG200	9491-F-0778 to 9491-F-0804
DG201	9491-F-0805 to 9491-F-0813
DG501	9491-F-1138 to 9491-F-1146
DG503	9491-F-1147 to 9491-F-1155
DG506	9491-F-1165 to 9491-F-1173
DG507	9491-F-1174 to 9491-F-1182
DG508	9491-F-1183 to 9491-F-1191
DG509	9491-F-1192 to 9491-F-1200
SI3705	9491-F-1156 to 9491-F-1164

For a detailed specification on any of these parts, contact Siliconix Ltd., Morriston, Swansea SA6 6NE
Telephone (0792) 74681 Telex: 48197

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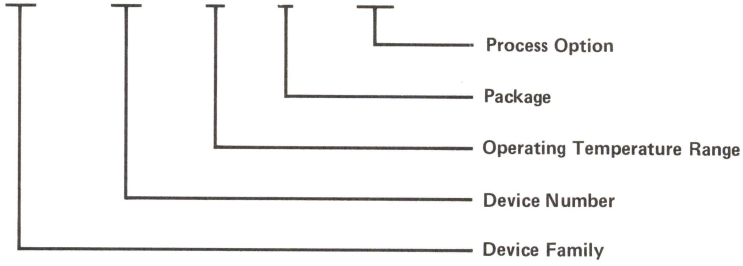
Device Ordering Information

DG	187	A	P	/883
DG	303	B	P	–4
DG	506	C	J	



DEVICE FAMILY
(1, 2 or 3 Letters)

D – Drivers for FET Switches
DG – Analog Switches
DGM – Analog Switches
G – Multi-Channel FETs
Si – Siliconix Second Source Part
SJM – QPL Listed Part

DEVICE NUMBER
(3 or 4 Digit Numbers)

OPERATING TEMPERATURE RANGE
(1 Letter)

A – –55 to 125°C
B – –20 to 85°C
C – 0 to 70°C

B temperature range parts receive industrial processing unless a process option dash number is added to the part number.

C temperature range parts are given commercial processing.

All possible combinations of device types, temperature ranges, package types and MIL-883 process options are not necessarily available. Consult individual data book pages for complete information.

PACKAGE
(1 Letter)

A – Metal Can
J – Dual In-Line Package – Plastic
K – Dual In-Line Package – CERDIP
L – Flat Package
P – Dual In-Line Package – Side Braze
R – Dual In-Line Package – Side Braze

PROCESS OPTION

/883 MIL-STD 883, Class B
–4 160 Hour Burn-In
BS9000 Series

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Analog Switches 1
Drivers for FET Switches 2
Multi-Channel FETs 3
Die Process and Topography Information 4
Burn-In Pin Connections 5
Mechanical Data 6
Appendices 7

2-Channel Monolithic SPST PMOS Switch with Driver

Siliconix

designed for . . .

- **Communication Systems**
- **Portable, Battery Operated Units**
- **Make-Before-Break Switching i.e. Feedback Resistor Switching in Variable Gain Op-Amps**
- **Sample and Hold Circuits**

BENEFITS

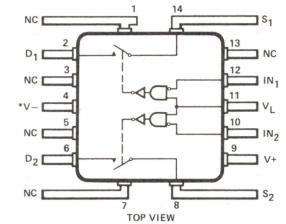
- **Minimizes Standby Power Requirements**
  - 550 μW
- **Low Leakage**
  - $\leqslant$ 1 nA
- **Reduces External Component Requirements**
  - Internal Zener Diodes Protect all MOS Gates

DESCRIPTION

These switching circuits contain two channels in one package; each channel consists of a driver circuit controlling an SPST MOS FET switch. The driver interfaces with DTL, TTL, or RTL logic signals for multiplexing, commutating, and D/A converter applications. Logic "0" at the input turns the FET switch ON, and logic "1" turns it OFF. Switches have make-before-break action.

PIN CONFIGURATIONS

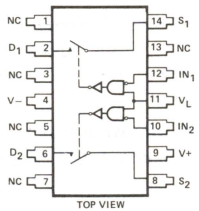
Flat Package



ORDER NUMBER: DGM111AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

Dual-In-Line Package

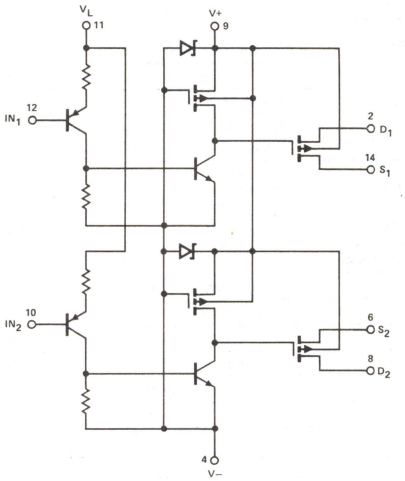


ORDER NUMBERS: DGM111AP OR DGM111BP
SEE PACKAGE 11

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

LOGIC	SWITCH
0	ON
1	OFF

SCHEMATIC DIAGRAM



APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S Analog Voltage Range (V)
10**	–20	5	4.6/0.8	–10 to +10
15	–15	5	4.6/0.8	–5 to +15
20	–10	5	4.6/0.8	0 to +20
+5	–15	5	4.6/0.8	–5 to +5

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics are based on V+ = +10 V, V– = 20 V only.

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ABSOLUTE MAXIMUM RATINGS

V+ to V− . . . . . 36 V
V+ to V_D or V_S . . . . . −0.5, 25 V
V_S to V− . . . . . 36 V
V_D to V− . . . . . 36 V
V_S to V_D . . . . . ±25 V
V_L to V− . . . . . 30 V
V_L to V_{IN} . . . . . ±6 V
Current (Any Terminal) . . . . . 30 mA
Storage Temperature . . . . . −65 to 150°C

Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
Power Dissipation*
Flat Package** . . . . . 750 mW
14 Pin DIP*** . . . . . 825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C
***Derate 11 mW/°C above 75°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

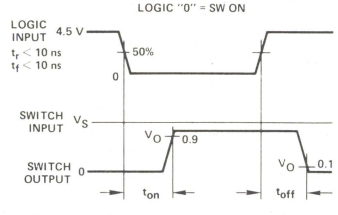
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_L = 4.5 V	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	75	75	115	75	75	100	Ω	V_D = 10 V	I_S = −1 mA, V_{IN} = 0.5 V
2				100	100	150	115	115	150		V_D = 0	
3				200	200	300	250	250	300		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		−1	−1,000		−5	−100	nA	V_S = −10 V, V_D = 10 V	V_{IN} = 4.1 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−1	−1,000		−5	−100		V_D = −10 V, V_S = 10 V	
6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		1	1,000		5	100		$V_D = V_S$ = 10 V	V_{IN} = 0.5 V
7	IN	I_{INL}	Logic Input Current, Input Voltage Low	−0.7	−0.7	−0.7	−1	−1	−1	mA	V_{IN} = 0.5 V	
8		I_{INH}	Logic Input Current, Input Voltage High	±1	±1	±10	±10	±10	±10	μA	V_{IN} = 4.1 V	
9	DYNAMIC	t_{on}	Turn-ON Time		0.3			0.3		μs	See Switching Time Test Circuit	
10		t_{off}	Turn-OFF Time		1			1				
11		$C_{S(off)}$	Source OFF Capacitance		5 Typ*			5 Typ*		pF	V_S = 0, I_D = 0	f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance		5 Typ*			5 Typ*			V_D = 0, I_S = 0	
13		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		16 Typ*			16 Typ*			$V_D = V_S$ = 0	
14		Off Isolation		Typ > −50 dB at 5 MHz*							R_L = 100Ω, C_L = 3 pF	
15	SUPPLY	I+	Positive Supply Current		3			3.5		mA	V_{IN} = 0.5 V, One Channel ON	
16		I−	Negative Supply Current		−4.5			−5				
17		I_L	Logic Supply Current		1.5			2				
18		I+	Positive Supply Current		10			10		μA	V_{IN} = 4.1 V, All Channels OFF	
19		I−	Negative Supply Current		−20			−20				
20		I_L	Logic Supply Current		10			10				

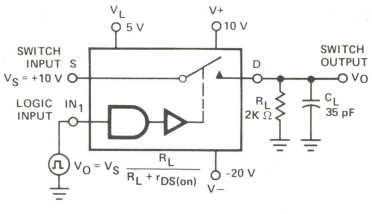
*Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

CMBG

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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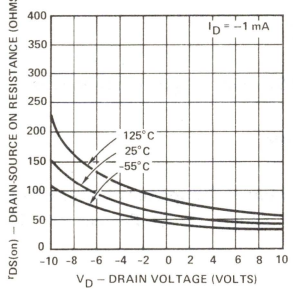
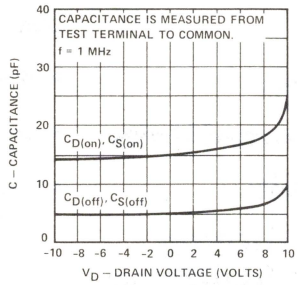
TYPICAL CHARACTERISTICS

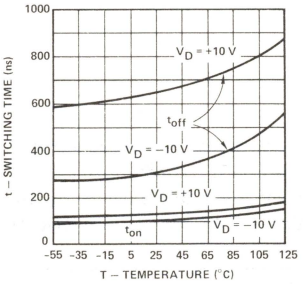
$r_{DS(on)}$ vs V_D and Temperature



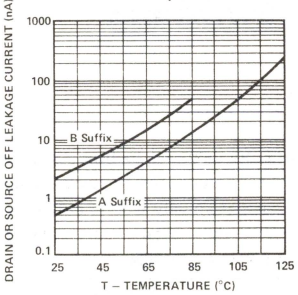
Capacitance vs V_D


CAPACITANCE IS MEASURED FROM TEST TERMINAL TO COMMON.
f = 1 MHz
$C_{D(on)}$, $C_{S(on)}$
$C_{D(off)}$, $C_{S(off)}$
C – CAPACITANCE (pF)
V_D – DRAIN VOLTAGE (VOLTS)

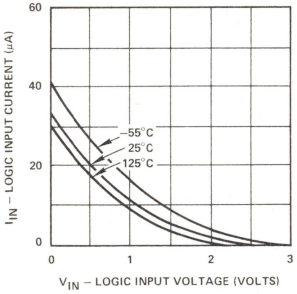
Switching Time vs V_D and Temperature



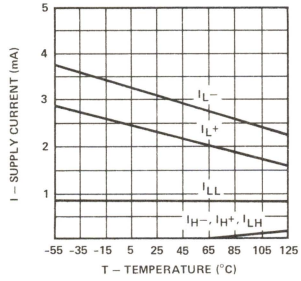
$I_{D(off)}/I_{S(off)}$ vs Temperature



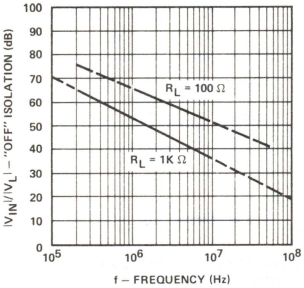
Input Current vs Input Voltage and Temperature

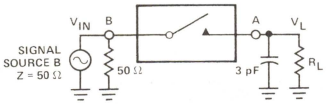


Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency

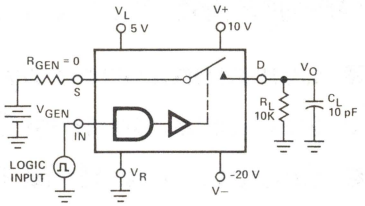




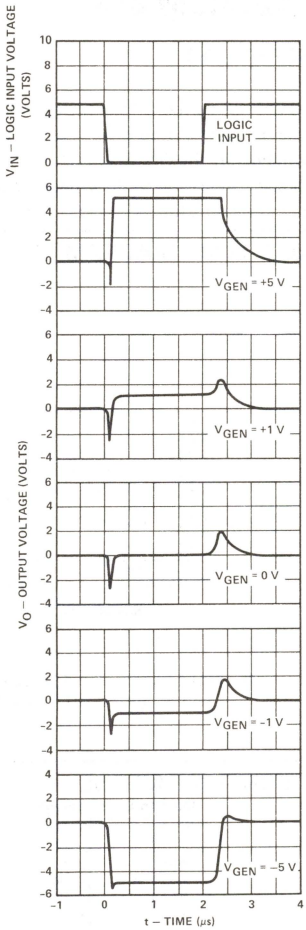
"OFF" ISOLATION ≙ 20 LOG $\frac{|V_{IN}|}{|V_L|}$

A – DRAIN OF "OFF" SWITCH
B – SOURCE OF "OFF" SWITCH

Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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2-Channel Monolithic DPST PMOS Switch with Driver

Siliconix

designed for . . .

- **Communication Systems**
- **Portable, Battery Operated Units**
- **Sample and Hold Circuits**
- **Make-Before-Break Switching i.e. Feedback Resistor Switching in Variable Gain Op-Amps**
- **DPST for Higher CMRR Switching Applications**

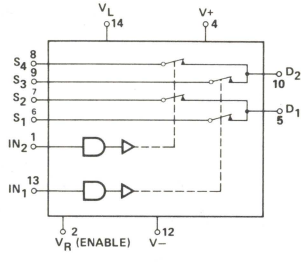
BENEFITS

- **Minimizes Standby Power Requirements**
  - 550 μW
- **Low Leakage**
  - $\leqslant$ 1 nA
- **Reduces External Component Requirements**
  - Internal Zener Diodes Protect all MOS Gates

DESCRIPTION

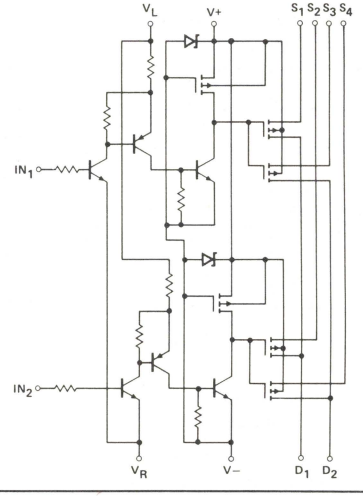
The DGM122 contains four MOS field-effect transistors designed to function as electronic switches. They are connected in pairs with level-shifting drivers which enable a low-level input (0.4 to 1.3 V) to control the ON-OFF condition of each pair of switches. In the ON state each switch conducts current equally well in either direction, and in the OFF state the switches will block voltages up to 20 V peak-to-peak. In the OFF state, total circuit power dissipation is < 0.5 mW. Positive logic "1" at the input turns the switch ON. Switch action is make-before break.

FUNCTIONAL DIAGRAM



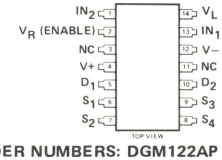
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

SCHEMATIC DIAGRAM



PIN CONFIGURATIONS

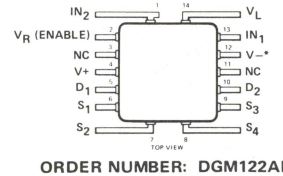
Dual-In-Line Package



ORDER NUMBERS: DGM122AP OR DGM122BP
SEE PACKAGE 11

LOGIC	SWITCH
0	OFF
1	ON

Flat Package



ORDER NUMBER: DGM122AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

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Siliconix

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V_D to V−	36 V
V_S to V−	36 V
V_D to V_S	±25 V
V_L to V−	25 V
V_R to V−	25 V
V_L to V_{IN}	6 V
V_R to V_{IN}	6 V
V_{IN} to V_R	2 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C

Power Dissipation*

Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

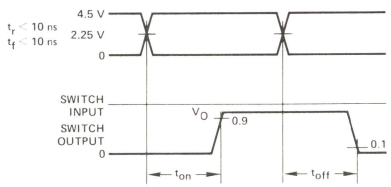
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

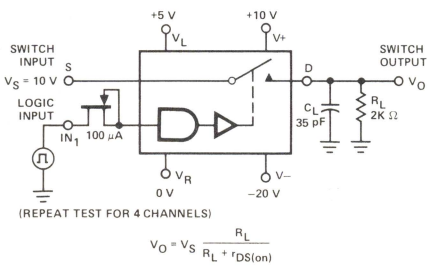
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	MAX LIMITS A SUFFIX 25°C	MAX LIMITS A SUFFIX 125°C	MAX LIMITS B SUFFIX −20°C	MAX LIMITS B SUFFIX 25°C	MAX LIMITS B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_L = 4.5 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_D = 10 V	I_S = −1 mA, I_{IN} = 100 μA
2				200	200	250	225	225	300		V_D = 0	
3				450	450	600	500	500	600		V_D = −10 V	
4		$\Delta r_{DS(on)}$	Resistance Difference Between Differential Switches		40			50			V_D = −10 V, I_S = −1.0 mA	
5		$I_{S(off)}$	Source OFF Leakage Current		−1	−1000		−5	−100	nA	V_S = −10 V, V_D = 10 V	V_{IN} = 0.4V
6		$I_{D(off)}$	Drain OFF Leakage Current		−3	−3000		−10	−300		V_D = −10 V, V_S = 10 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		3	3000		10	300		V_D = 10 V, I_S = 0	I_{IN} = 100 μA
8	IN	I_{INL}	Logic Input Current, Input Voltage Low	1	1		10	10		μA	V_{IN} = 0.4 V	
9						1			10		V_{IN} = 0.3 V	
10		V_{INH}	Input Voltage, High	1.3	1.3	1	1.3	1.3	1.3	V	I_{IN} = 100 μA	
11	DYNAMIC	t_{on}	Turn-ON Time		0.3			0.5		μs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		2			2				
13		$C_{S(off)}$	Source OFF Capacitance		5 Typ*			5 Typ*		pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance		9 Typ*			9 Typ*			V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel On Capacitance		17 Typ*			17 Typ*			V_D = V_S = 0	
16		Off Isolation		Typ > −50 dB at 5 MHz*							R_L = 100Ω, C_L = 3 pF	
17	SUPPLY	I+	Positive Supply Current		3			3		mA	I_{IN} = 100 μA, One Channel ON	
18		I−	Negative Supply Current		−6			−6				
19		I_L	Logic Supply Current		3			3				
20		I_R	Reference Supply Current		−1.5			−1.5				
21		I+	Positive Supply Current		10			20		μA	V_{IN} = 0.4 V, All Channels OFF	
22		I−	Negative Supply Current		−20			−40				
23		I_L	Logic Supply Current		10			20				
24		I_R	Reference Supply Current		−15			−25				

*Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

CMBA

SWITCHING TIME TEST CIRCUIT





$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

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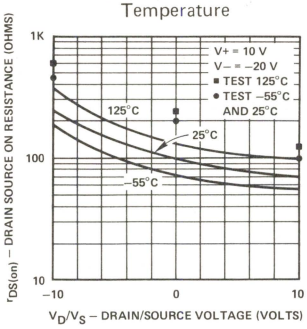
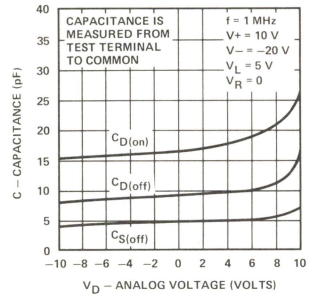
TYPICAL CHARACTERISTICS

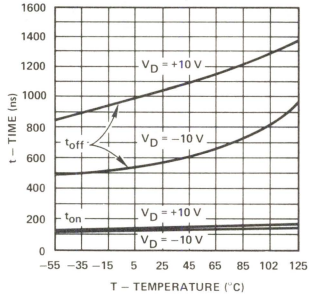
$r_{DS(on)}$ vs V_D and Temperature



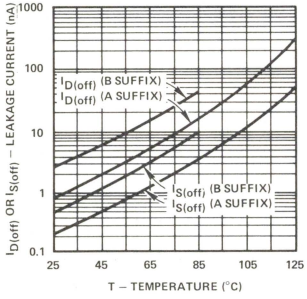
Capacitance vs V_D



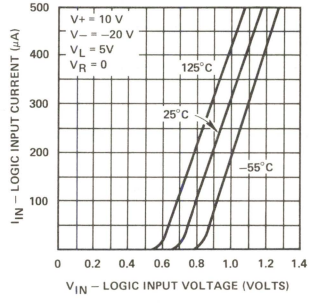
Switching Time vs V_D and Temperature



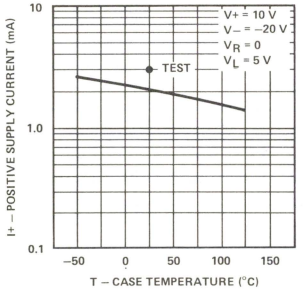
$I_{D(off)}/I_{S(off)}$ vs Temperature



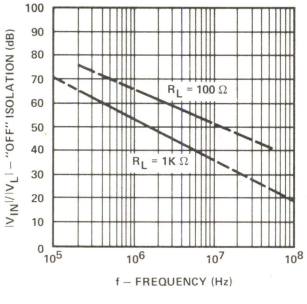
I_{IN} vs V_{IN} and Temperature

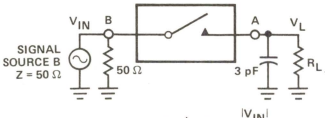


Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency

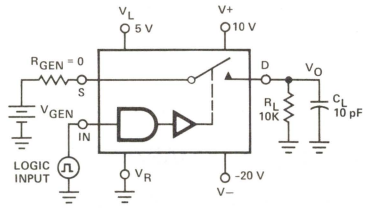




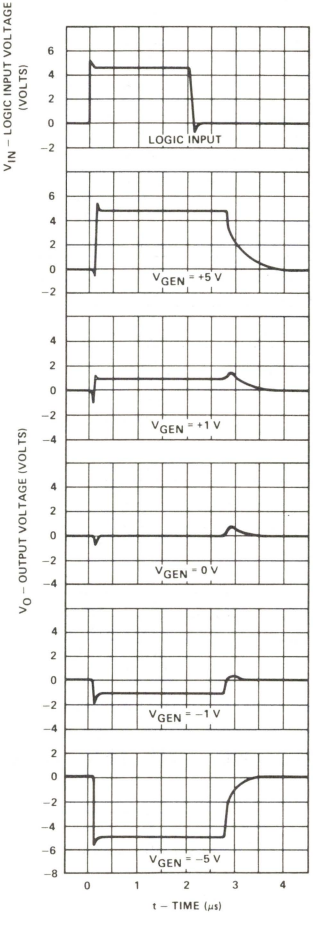
"OFF" ISOLATION ≙ 20 LOG $\frac{|V_{IN}|}{|V_L|}$

A – DRAIN OF "OFF" SWITCH
B – SOURCE OF "OFF" SWITCH

Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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5-Channel SPST PMOS Switches with Drivers

Siliconix

designed for . . .

- **Communication Systems**
- **Portable, Battery Operated Units**
- **Make-Before-Break Switching i.e. Feedback Resistor Switching in Variable Gain Op-Amps**

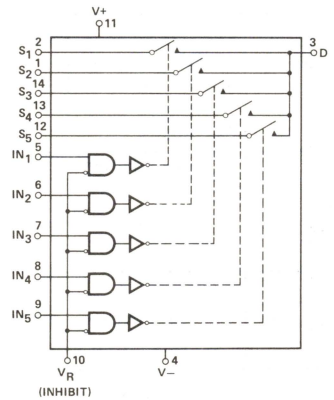
BENEFITS

- **Minimizes Standby Power Requirements**
  - 550 μW
- **Low Leakage**
  - $\leqslant$ 1 nA
- **Reduces External Component Requirements**
  - Internal Zener Diodes Protect All MOS Gates

DESCRIPTION

The DG123 contains five MOS field-effect transistors designed to function as electronic switches. Level-shifting drivers enable a low-level input (0.4 to 1.3 V) to control the ON-OFF condition of each switch. In the ON state each switch conducts current equally well in either direction, and in the OFF state the switches will block voltages up to 20 V peak-to-peak. In the OFF state, total circuit power dissipation is $<$ 0.5 mW. Positive logic "1" at the input turns the switch ON. Switch action is make-before-break.

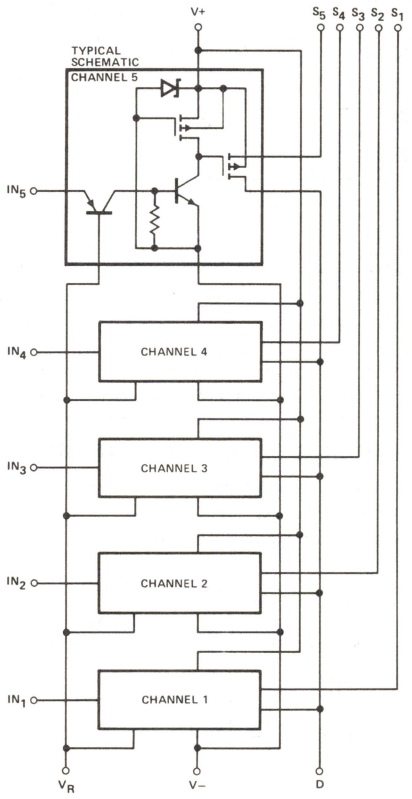
FUNCTIONAL DIAGRAM



LOGIC	SWITCH
0	ON
1	OFF

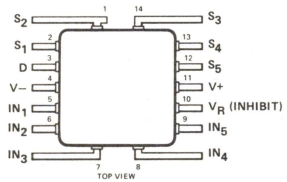
SWITCHES CLOSED FOR LOGIC "1" INPUT
(POSITIVE LOGIC)

SCHEMATIC DIAGRAM



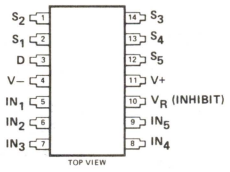
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER:
DG123AL
SEE PACKAGE 5

Dual-In-Line Package



ORDER NUMBERS:
DG123AP OR DG123BP
SEE PACKAGE 11

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ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V_D to V−	36 V
V_S to V−	36 V
V_D to V_S	25 V
V_S to V_D	25 V
V_R to V−	30 V
V_{IN} to V−	30 V
V_R to V_{IN}	6 V
V_{IN} to V_R	2 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

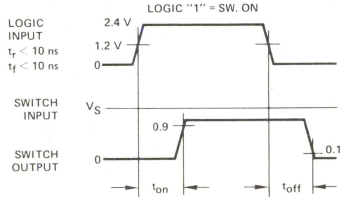
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	25°C	125°C	MAX LIMITS B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_D = 10 V	I_S = −1 mA, I_{IN} = 1 mA
2				200	200	250	225	225	300		V_D = 0	
3				450	450	600	500	500	600		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		−1	−1000		−5	−100	nA	V_S = −10 V, V_D = 10 V	V_{IN} = 0.4 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−1	4000		−10	−300		V_D = −10 V, V_S = 10 V	
6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		4	4000		10	300		$V_D = V_S$ = 10 V	I_{IN} = 1 mA
7	IN	I_{INL}	Logic Input Current, Input Voltage Low	1	1	100	5	5	100	μA	V_{IN} = 0.4 V	
8		V_{INH}	Input Voltage, High	1.3	1	0.8	1.3	1	1	V	I_{IN} = 1 mA	
9	DYNAMIC	t_{on}	Turn-ON Time		0.3			0.5		μs	See Switching Time Test Circuit	
10		t_{off}	Turn-OFF Time		2			2				
11		$C_{S(off)}$	Source OFF Capacitance		3 Typ*			3 Typ*		pF	V_S = 0, I_D = 0	f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance		7 Typ*			7 Typ*			V_D = 0, I_S = 0	
13		Off Isolation		Typ > −50 dB at 5 MHz*							R_L = 100Ω, C_L = 3 pF	
14	SUPPLY	I+	Positive Supply Current		3			3		mA	I_{IN} = 1 mA, One Channel ON	
15		I−	Negative Supply Current		−6			−6				
16		I_R	Reference Supply Current		−0.5			−0.5				
17		I+	Positive Supply Current		15			25		μA	V_{IN} = 0.4 V, All Channels OFF	
18		I−	Negative Supply Current		−20			−40				
19		I_R	Reference Supply Current		−10			−20				

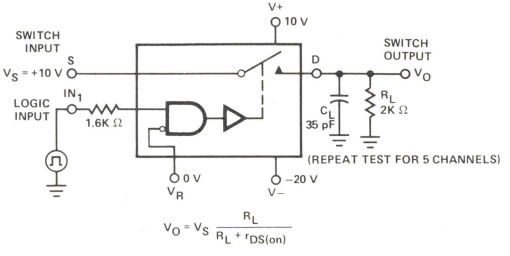
*Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

EIDB + MABA

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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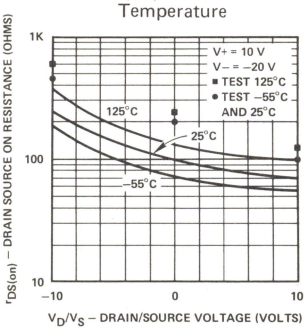
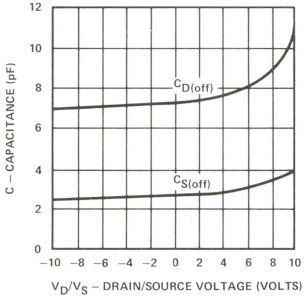
TYPICAL CHARACTERISTICS

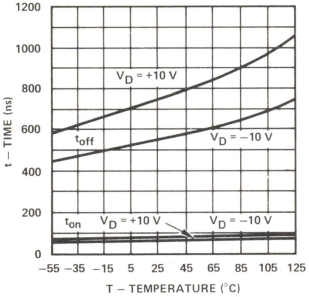
$r_{DS(on)}$ vs V_D and Temperature



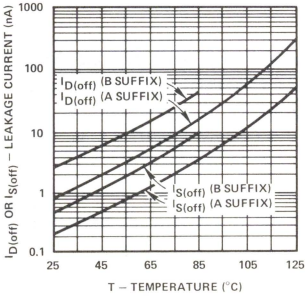
Capacitance vs V_D



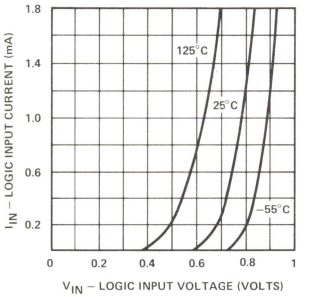
Switching Time vs V_D and Temperature



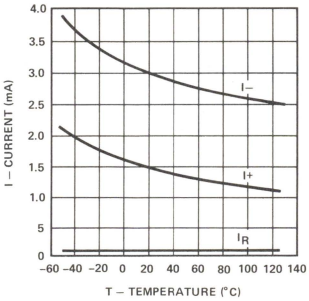
$I_{D(off)}/I_{S(off)}$ vs Temperature



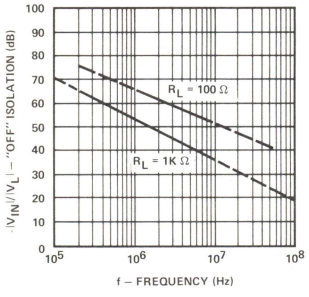
I_{IN} vs V_{IN} and Temperature

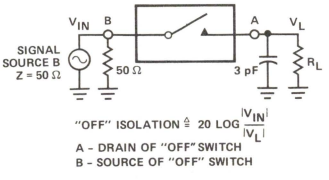


Supply Current vs Temperature

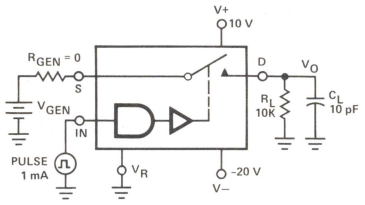


"OFF" Isolation vs R_L and Frequency

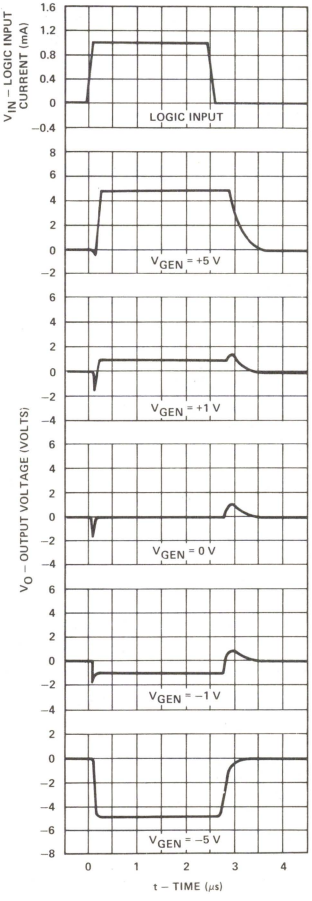




Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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5-Channel SPST PMOS Switches with Drivers

Siliconix

designed for . . .

- **Communication Systems**
- **Portable, Battery Operated Units**
- **Make-Before-Break Switching i.e. Feedback Resistor Switching in Variable Gain Op-Amps**

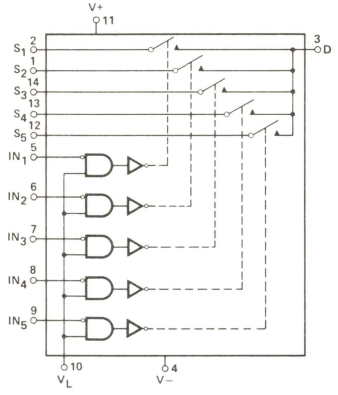
BENEFITS

- **Minimizes Standby Power Requirements**
  - 550 μW
- **Low Leakage**
  - $\leqslant$ 1 nA
- **Reduces External Component Requirements**
  - Internal Zener Diodes Protect All MOS Gates

DESCRIPTION

The DG125 contains five MOS field-effect transistors designed to function as electronic switches. Level-shifting drivers enable a low-level input (0.4 to 5 V) to control the ON-OFF condition of each switch. In the ON state each switch conducts current equally well in either direction, and in the OFF state the switches will block voltages up to 20 V peak-to-peak. In the OFF state, total circuit power dissipation is < 0.5 mW. Positive logic "1" at the input turns the switch OFF. Switch action is make-before-break.

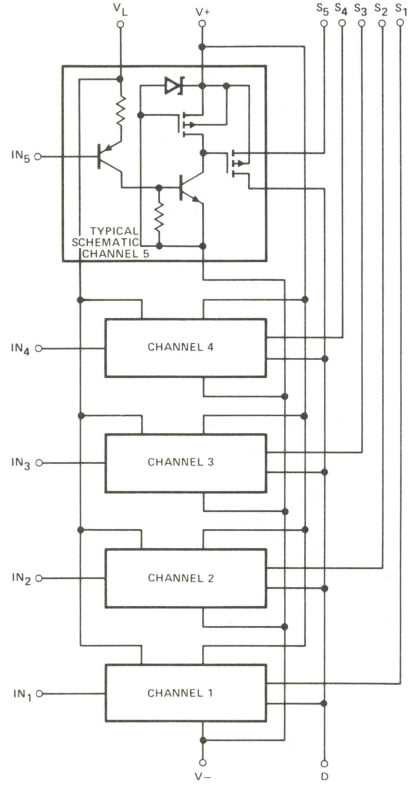
FUNCTIONAL DIAGRAM



LOGIC	SWITCH
0	ON
1	OFF

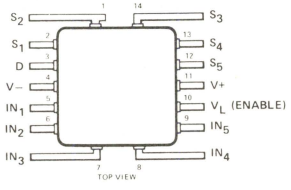
SWITCH STATES ARE FOR LOGIC "1" INPUT
(POSITIVE LOGIC)

SCHEMATIC DIAGRAM



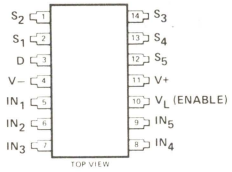
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER: DG125AL
SEE PACKAGE 5

Dual-In-Line Package



ORDER NUMBERS:
DG125AP OR DG125BP
SEE PACKAGE 11

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Siliconix

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V_D to V−	36 V
V_S to V−	36 V
V_D to V_S	25 V
V_S to V_D	25 V
V_L to V−	30 V
V_{IN} to V−	30 V
V_L to V_{IN}	6 V
Current (Any Terminal)	30 mA

Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

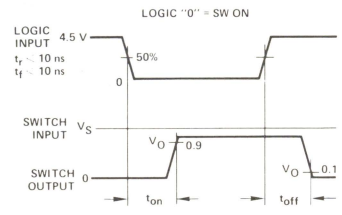
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_L = 4.5 V	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	100	100	125	125	125	150	Ω	V_D = 10 V	I_S = −1 mA, V_{IN} = 0.5 V
2				200	200	250	225	225	300		V_D = 0	
3				450	450	600	500	500	600		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		−1	−1000		−5	−100	nA	V_S = −10 V, V_D = 10 V	V_{IN} = 4.1 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−1	−4000		−10	−300		V_D = −10 V, V_S = 10 V	
6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		4	4000		10	300		V_D = 10 V, I_S = 0	V_{IN} = 0.5 V
7	IN	I_{INL}	Logic Input Current, Input Voltage Low	−0.7	−0.7	−0.7	−1	−1	−1	mA	V_{IN} = 0.5 V	
8		I_{INH}	Logic Input Current, Input Voltage High	±1	±1	±10	±10	±10	±10	μA	V_{IN} = 4.1 V	
9	DYNAMIC	t_{on}	Turn-ON Time		0.3			0.5		μs	See Switching Time Test Circuit	
10		t_{off}	Turn-OFF Time		2			2				
11		$C_{S(off)}$	Source OFF Capacitance		3 Typ*			3 Typ*		pF	V_S = 0, I_D = 0	f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance		7 Typ*			7 Typ*			V_D = 0, I_S = 0	
13		Off Isolation		Typ > −50 dB at 5 MHz*							R_L = 100Ω, C_L = 3 pF	
14	SUPPLY	I+	Positive Supply Current		3			3		mA	V_{IN} = 0.5 V, One Channel ON	
15		I−	Negative Supply Current		−6			−6				
16		I_L	Logic Supply Current		3			3				
17		I+	Positive Supply Current		15			25		μA	V_{IN} = 4.1 V, All Channels OFF	
18		I−	Negative Supply Current		−20			−40				
19		I_L	Logic Supply Current		10			20				

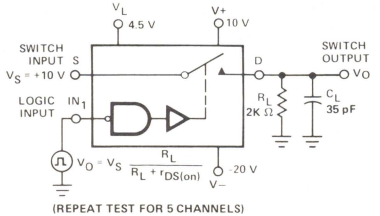
*Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

BID + MABA

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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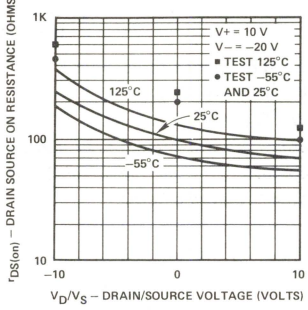
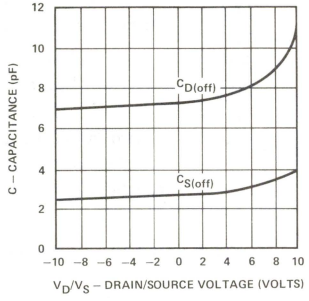
TYPICAL CHARACTERISTICS

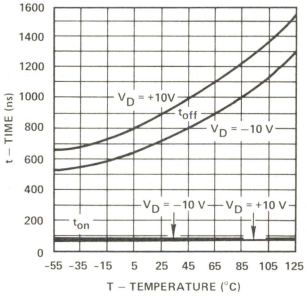
$r_{DS(on)}$ vs V_D and Temperature



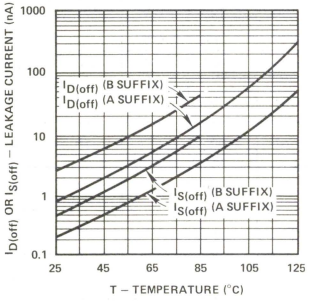
Capacitance vs V_D



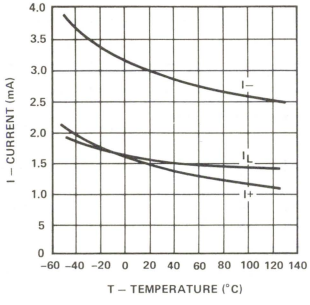
Switching Time vs V_D and Temperature



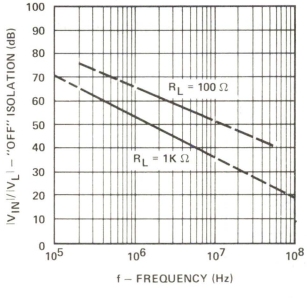
$I_{D(off)}/I_{S(off)}$ vs Temperature

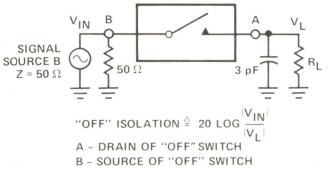


Supply Current vs Temperature

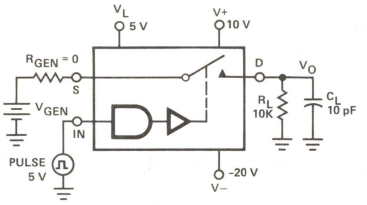


"OFF" Isolation vs R_L and Frequency

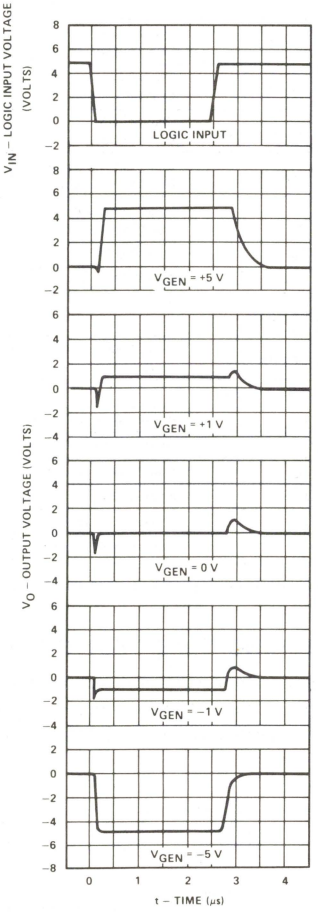




Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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2-Channel Drivers with SPST and DPST FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

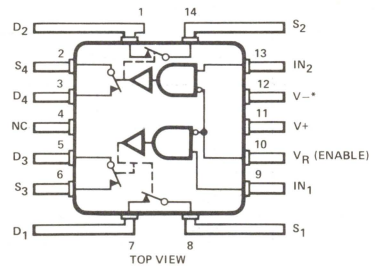
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

These switching circuits contain two channels in one package; each channel consists of a driver circuit controlling SPST or DPST junction FET switches. The driver interfaces with DTL, TTL or RTL logic signals for multiplexing, commutating, and D/A converter applications. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF. Switches have make-before-break action. It is recommended that the DG185 and DG182 be used for new designs.

PIN CONFIGURATIONS

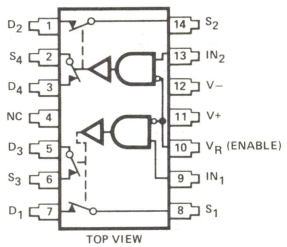
Flat Package



TOP VIEW

ORDER NUMBER:
DG126AL
SEE PACKAGE 5

Dual-In-Line Package

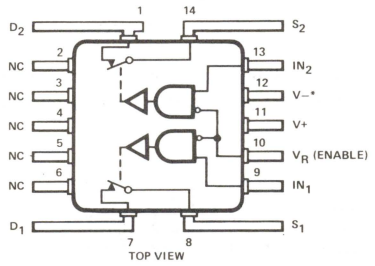


TOP VIEW

ORDER NUMBERS:
DG126AP OR DG126BP
SEE PACKAGE 11

LOGIC	SWITCH
0	OFF
1	ON

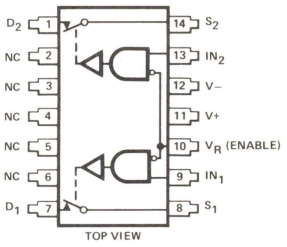
Flat Package



TOP VIEW

ORDER NUMBER:
DG134AL
SEE PACKAGE 5

Dual-In-Line Package



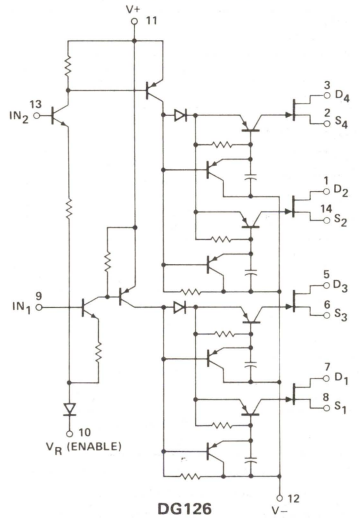
TOP VIEW

ORDER NUMBERS:
DG134AP OR DG134BP
SEE PACKAGE 11

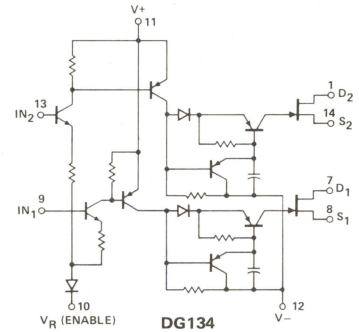
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR LOGIC "1" INPUT

SCHEMATIC DIAGRAMS



DG126



DG134

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ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	36 V
V_D or V_S to V−	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V_R to V−	25 V
V_{IN} to V−	30 V
V+ to V_{IN}	25 V
V_{IN} to V_R	±6 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C

Power Dissipation*

Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

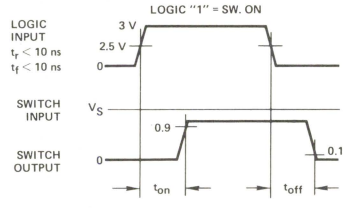
		CHARACTERISTIC		MAX LIMITS DG126A, DG134A −55°C	25°C	125°C	MAX LIMITS DG126B, DG134B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	80	80	150				Ω	V_D = 10 V	I_S = −10 mA, V_{IN} = 2.5 V*
2							100	100	150		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 10 V, V_D = −10 V	V_{IN} = 0.8 V*
4								5	100		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 10 V, V_S = −10 V	
6								5	100		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN} = 2.5 V*
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN} = 0.8 V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		V_{IN} = 2.5 V*	
11	DYNAMIC	t_{on}	Turn-ON Time		0.6			1		μs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		1.6			2				
13		$C_{S(off)}$	Source OFF Capacitance	2.4 Typical**						pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance	2.4 Typical**							V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	2.8 Typical**							V_D = V_S = 0	
16		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
17	SUPPLY	I+	Positive Supply Current		3.0			3.3		mA	V_{IN} = 2.5 V, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2.0				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		μA	Both V_{IN} = 0*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

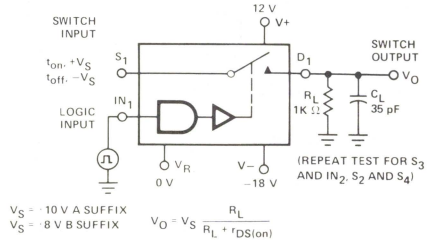
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODC + NC

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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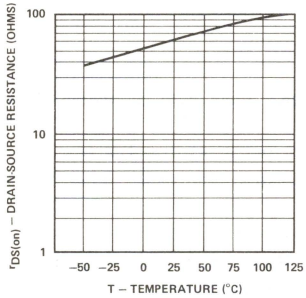
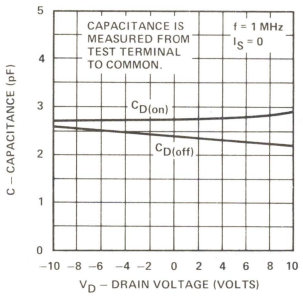
TYPICAL CHARACTERISTICS

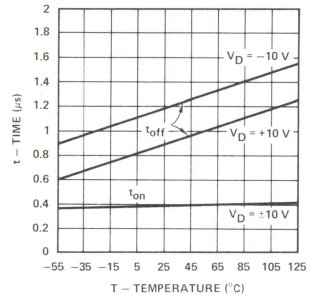
$r_{DS(on)}$ vs Temperature



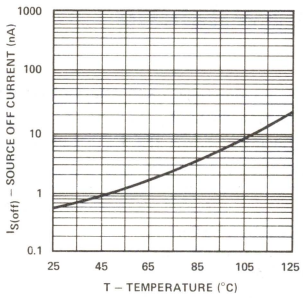
Capacitance vs V_D



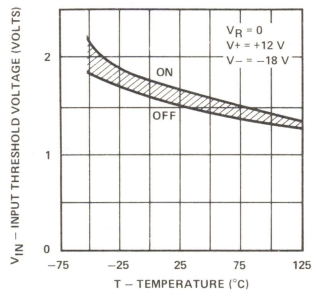
Switching Time vs V_D and Temperature



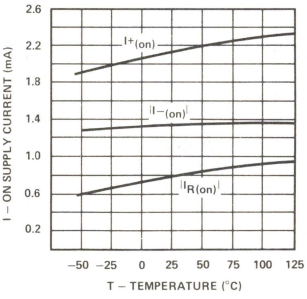
$I_{S(off)}$ vs Temperature



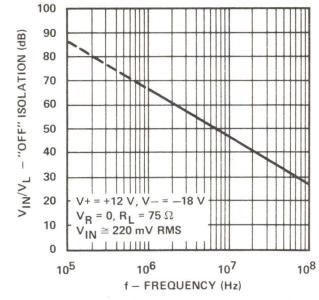
V_{IN} vs Temperature



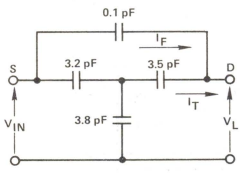
Supply Current vs Temperature



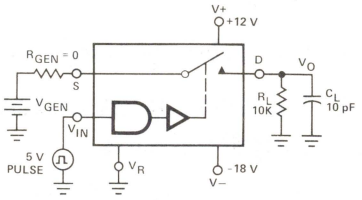
"OFF" Isolation vs R_L and Frequency



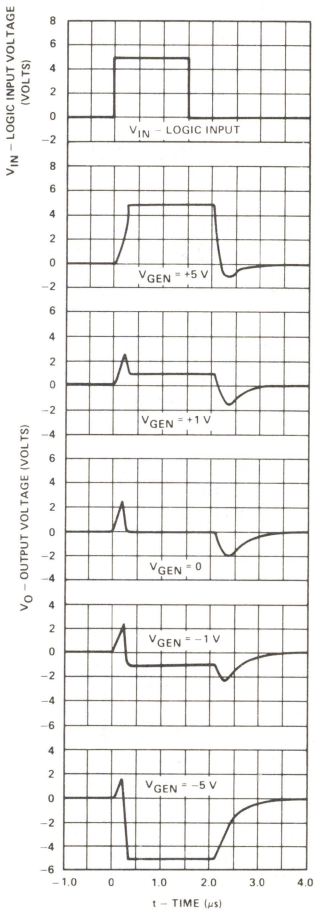
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


V_{IN} – LOGIC INPUT VOLTAGE (VOLTS)
V_{IN} – LOGIC INPUT
V_{GEN} = +5 V
V_{GEN} = +1 V
V_{GEN} = 0
V_{GEN} = –1 V
V_{GEN} = –5 V
V_O – OUTPUT VOLTAGE (VOLTS)
–1.0 0 1.0 2.0 3.0 4.0
t – TIME (μs)

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2-Channel Drivers with SPST and DPST FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

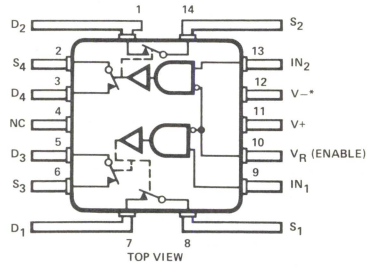
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

These switching circuits contain two channels in one package; each channel consists of a driver circuit controlling SPST or DPST junction FET switches. The driver interfaces with DTL, TTL or RTL logic signals for multiplexing, commutating, and D/A converter applications. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF. Switches have make-before-break action. It is recommended that the DG184 and DG181 be used for new designs.

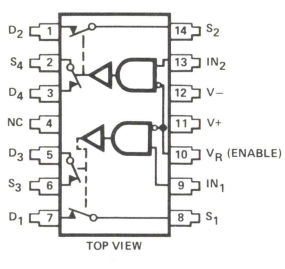
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER:
DG129AL
SEE PACKAGE 5

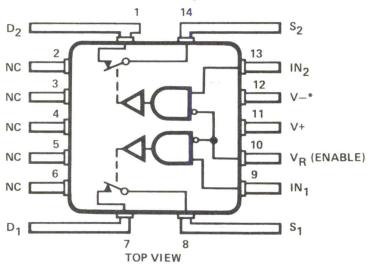
Dual-In-Line Package



ORDER NUMBERS:
DG129AP OR DG129BP
SEE PACKAGE 11

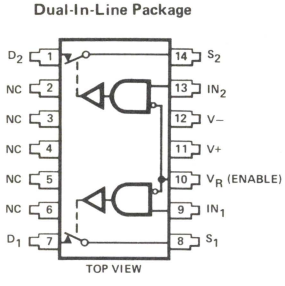
LOGIC	SWITCH
0	OFF
1	ON

Flat Package



ORDER NUMBER:
DG133AL
SEE PACKAGE 5

Dual-In-Line Package

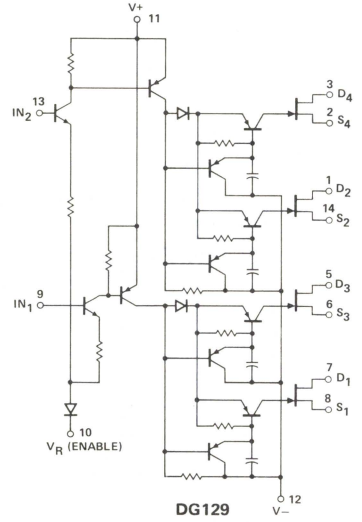


ORDER NUMBERS:
DG133AP OR DG133BP
SEE PACKAGE 11

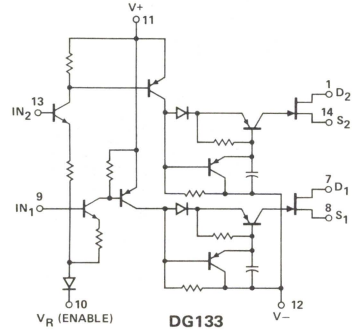
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR LOGIC "1" INPUT

SCHEMATIC DIAGRAMS



DG129



DG133

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Siliconix

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	36 V
V_D or V_S to V−	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V_R to V−	25 V
V_{IN} to V−	30 V
V+ to V_{IN}	25 V
V_{IN} to V_R	±6 V
Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS DG129A, DG133A −55°C	25°C	125°C	DG129B, DG133B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	30	30	60				Ω	V_D = 10 V	I_S = −10 mA, V_{IN} = 2.5 V*
2							50	50	75		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 10 V, V_D = −10 V	V_{IN} = 0.8 V*
4								5	100		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 10 V, V_S = −10 V	
6								5	100		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN} = 2.5 V*
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	µA	V_{IN} = 0.8 V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		V_{IN} = 2.5 V*	
11	DYNAMIC	t_{on}	Turn-ON Time		0.6			1		µs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		1.6			2				
13		$C_{S(off)}$	Source OFF Capacitance	2.4 Typical**						pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance	2.4 Typical**							V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	2.8 Typical**							V_D = V_S = 0	
16		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
17	SUPPLY	I+	Positive Supply Current		3.0			3.3		mA	V_{IN} = 2.5V*, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2.0				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		µA	Both V_{IN} = 0*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

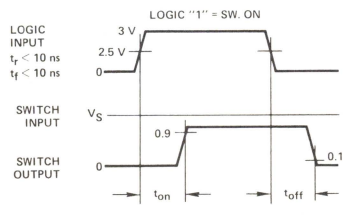
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/µs.

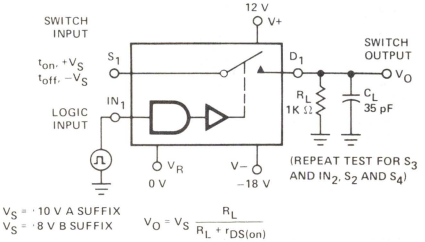
**Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODC + NC

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





V_S = ±10 V A SUFFIX
V_S = ±8 V B SUFFIX

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

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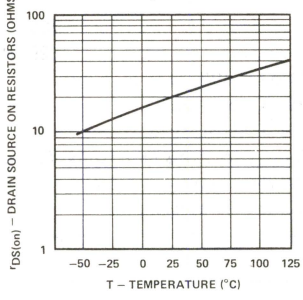
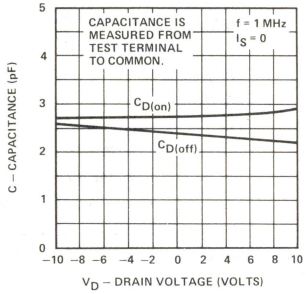
TYPICAL CHARACTERISTICS

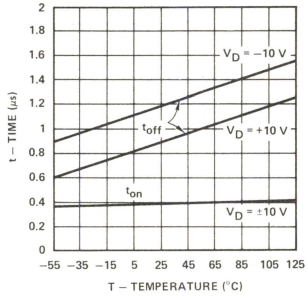
$r_{DS(on)}$ vs Temperature



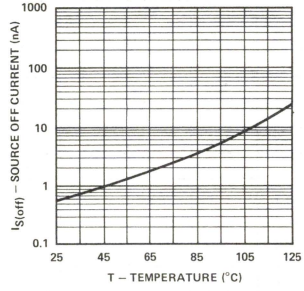
Capacitance vs V_D



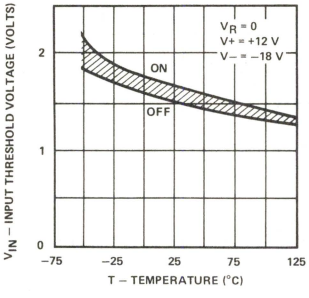
Switching Time vs V_D and Temperature



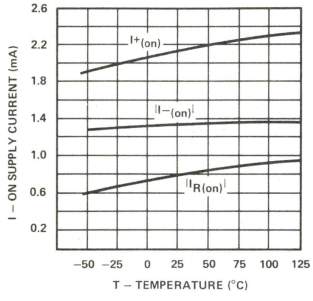
$I_{S(off)}$ vs Temperature



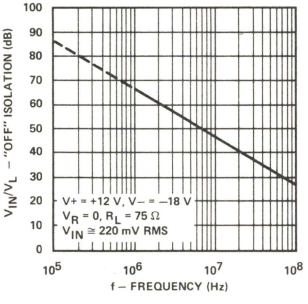
V_{IN} vs Temperature



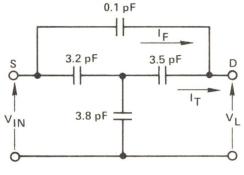
Supply Current vs Temperature



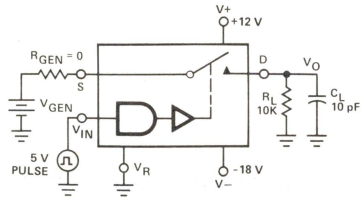
"OFF" Isolation vs R_L and Frequency



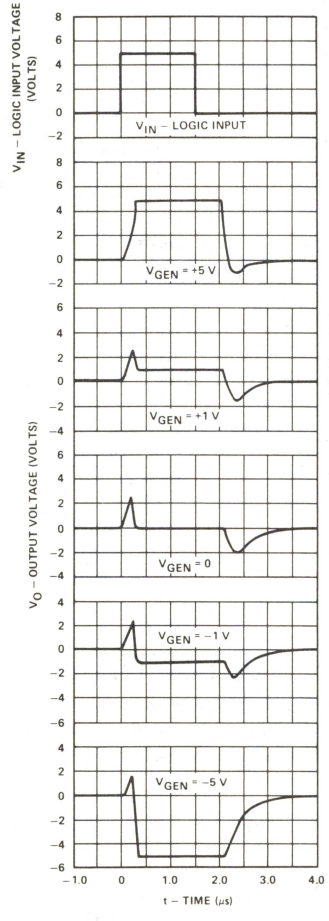
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


V_{IN} – LOGIC INPUT VOLTAGE (VOLTS)
V_{IN} – LOGIC INPUT
V_{GEN} = +5 V
V_{GEN} = +1 V
V_{GEN} = 0
V_{GEN} = –1 V
V_{GEN} = –5 V
V_O – OUTPUT VOLTAGE (VOLTS)
–1.0 0 1.0 2.0 3.0 4.0
t – TIME (μs)

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Drivers with Normally Open & Normally Closed FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

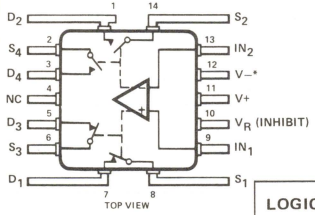
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

The DG139 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 30 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 20 V peak-to-peak. Switches have make-before-break action. The DG144 is similar to the DG139, except that it contains two FET switches instead of four. It is recommended that the DG190 and DG187 be used for new designs.

PIN CONFIGURATIONS

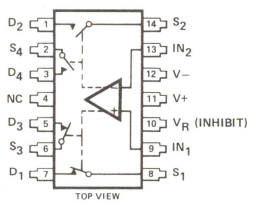
Flat Package



ORDER NUMBER:
DG139AL
SEE PACKAGE 5

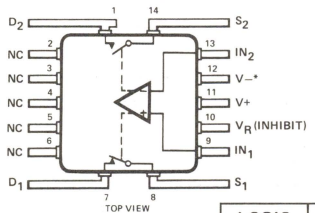
LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package



ORDER NUMBERS:
DG139AP OR DG139BP
SEE PACKAGE 11

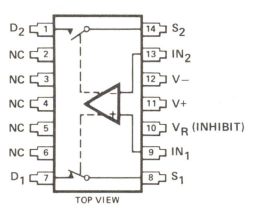
Flat Package



ORDER NUMBER:
DG144AL
SEE PACKAGE 5

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package

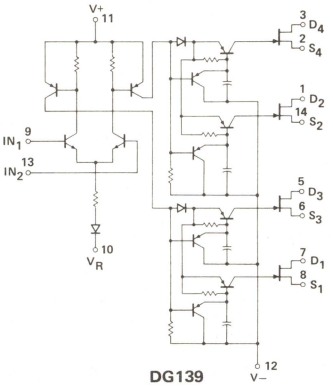


ORDER NUMBERS:
DG144AP OR DG144BP
SEE PACKAGE 11

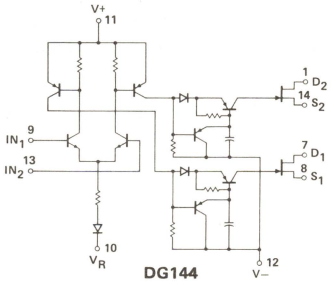
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR
V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS
(POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG139



DG144

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ABSOLUTE MAXIMUM RATINGS

V+ to V−, V_D or V_S	36 V
V_D or V_S to V−	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V
Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

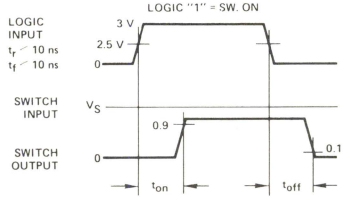
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0, V_{IN2} = 2.5 V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	30	30	60				Ω	V_D = 10 V	I_S = −10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							50	50	75		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 10 V, V_D = −10 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								5	100		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 10 V, V_S = −10 V	
6								5	100		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	µA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13	DYNAMIC	t_{on}	Turn-ON Time		0.8			1		µs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		1.6			2				
15		$C_{S(off)}$	Source OFF Capacitance		** 2.4 Typ			** 2.4 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		** 2.4 Typ			** 2.4 Typ			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel On Capacitance		** 2.8 Typ			** 2.8 Typ			V_D = V_S = 0	
18		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
19	SUPPLY	I+	Positive Supply Current		4.2			4.5		mA	V_{IN1} = 2 V* or V_{IN1} = 3 V*, One Channel ON	
20		I−	Negative Supply Current		−2			−2.2				
21		I_R	Reference Supply Current		−2.2			−2.4				
22		I+	Positive Supply Current		25			25		µA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I−	Negative Supply Current		−25			−25				
24		I_R	Reference Supply Current		−25			−25				

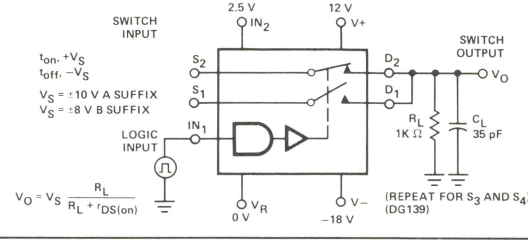
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/µs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODF + NC

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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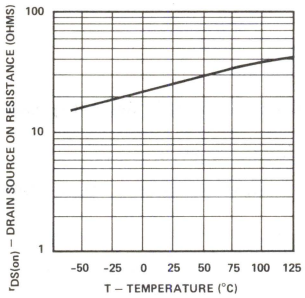
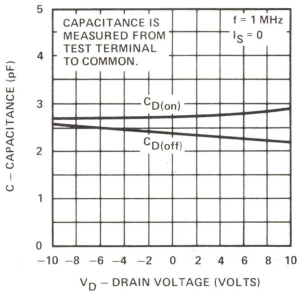
TYPICAL CHARACTERISTICS

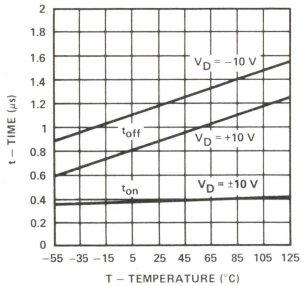
$r_{DS(on)}$ vs Temperature



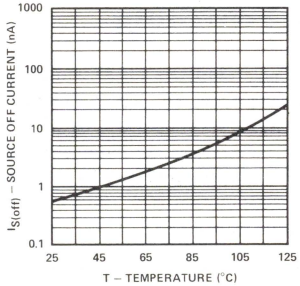
Capacitance vs V_D



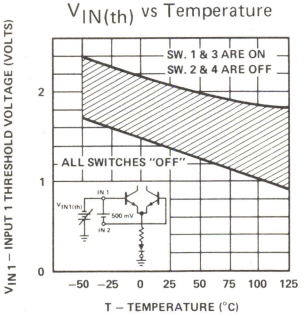
Switching Time vs V_D and Temperature



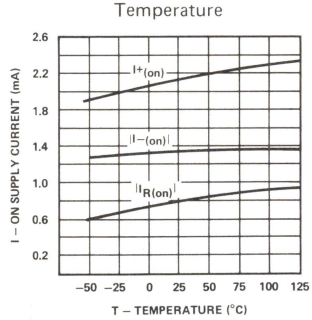
$I_{S(off)}$ vs Temperature



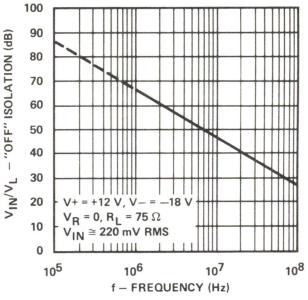
$V_{IN(th)}$ vs Temperature



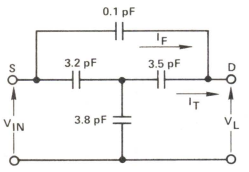
Supply Current vs Temperature



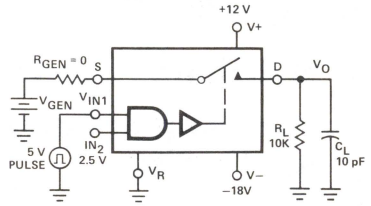
"OFF" Isolation vs R_L and Frequency



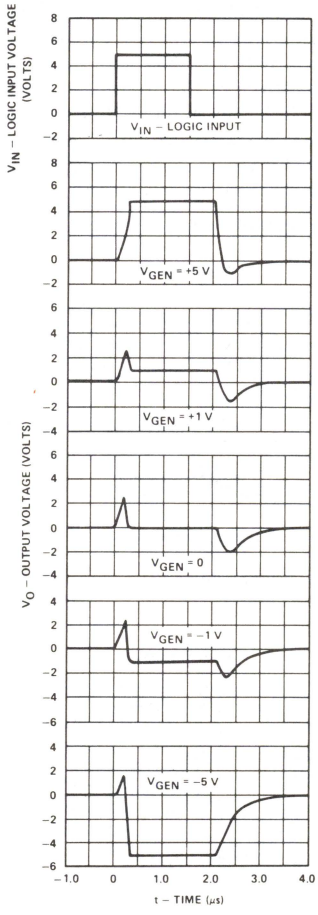
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


V_{IN} – LOGIC INPUT VOLTAGE (VOLTS)
V_{IN} – LOGIC INPUT
V_{GEN} = +5 V
V_{GEN} = +1 V
V_{GEN} = 0
V_{GEN} = −1 V
V_{GEN} = −5 V
V_O – OUTPUT VOLTAGE (VOLTS)
-1.0 0 1.0 2.0 3.0 4.0
t – TIME (µs)

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2-Channel Drivers with SPST and DPST FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

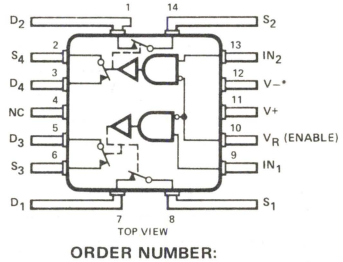
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

The DG140 contains four junction-type field-effect transistors (JFETs) designed to function as two double-pole single-throw electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With a positive logic "0" at the driver input the switches will be OFF. With a positive logic "1" at the input the switches will be ON. In the ON state each switch will conduct current in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. ON series resistance is < 10 ohms, and ON shunt leakage is < 2 nA. With both drivers in the "switch OFF" state total power consumption is < 750 μW. Switches have make-before-break action. The DG141 is similar to the DG140 except that it contains two SPST switch functions. It is recommended that the DG183 and DG180 be used for new designs.

PIN CONFIGURATIONS

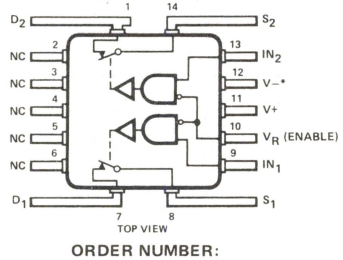
Flat Package



ORDER NUMBER:
DG140AL
SEE PACKAGE 5

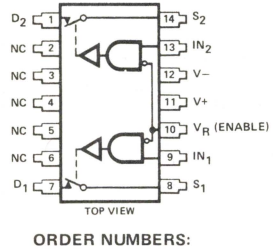
LOGIC	SWITCH
0	OFF
1	ON

Flat Package



ORDER NUMBER:
DG141AL
SEE PACKAGE 5

Dual-In-Line Package

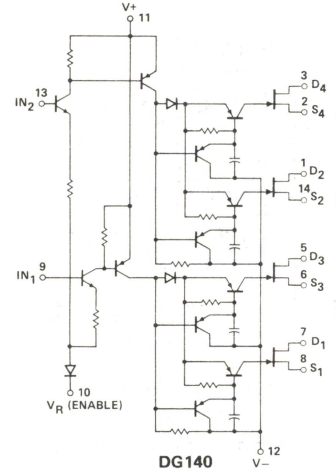


ORDER NUMBERS:
DG141AP OR DG141BP
SEE PACKAGE 11

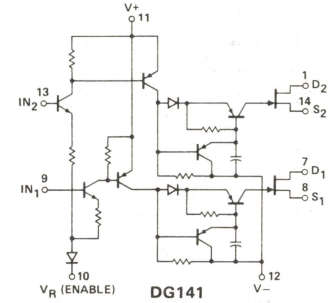
*Common to Substrate and Base of Package

SWITCH STATES ARE LOGIC "1" INPUT

SCHEMATIC DIAGRAMS



DG140



DG141

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Siliconix

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D or V_S	36 V
V_D or V_S to V−	32 V
V_D to V_S	±22 V
V+ to V_R	25 V
V_R to V−	25 V
V_{IN} to V−	30 V
V+ to V_{IN}	25 V
V_{IN} to V_R	±6 V
Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

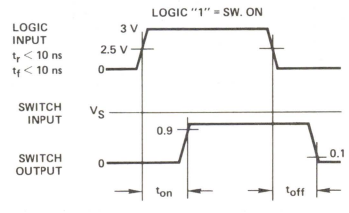
		CHARACTERISTIC		MAX LIMITS DG140A, DG141A −55°C	25°C	125°C	MAX LIMITS DG140B, DG141B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	10	10	20				Ω	V_D = 10 V	I_S = −10 mA, V_{IN} = 2.5 V*
2							15	15	25		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		10	1000				nA	V_S = 10 V, V_D = −10 V	V_{IN} = 0.8 V*
4								15	300		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		10	1000					V_D = 10 V, V_S = −10 V	
6								15	300		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					$V_D = V_S$ = −10 V	V_{IN} = 2.5 V*
8								−5	−100		$V_D = V_S$ = −8 V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	µA	V_{IN} = 0.8 V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		V_{IN} = 2.5 V*	
11	DYNAMIC	t_{on}	Turn-ON Time		1			1.5		µs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		2.5			2.5				
13		$C_{S(off)}$	Source OFF Capacitance		** 3 Typ			** 3 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance		** 3 Typ			** 3 Typ			V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		** 2.8 Typ			** 2.8 Typ			$V_D = V_S$ = 0	
16		Off Isolation		Typ > 50 dB at 1 MHz**							R_L = 100 Ω, C_L = 3 pF	
17	SUPPLY	I+	Positive Supply Current		3			3.3		mA	V_{IN} = 2.5 V*, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		µA	Both V_{IN} = 0*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

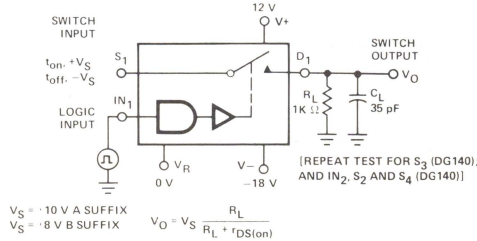
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/µs.
**Typical values are for DESIGN AID only, not guaranteed and not subject to production testing.

LODC + NIP

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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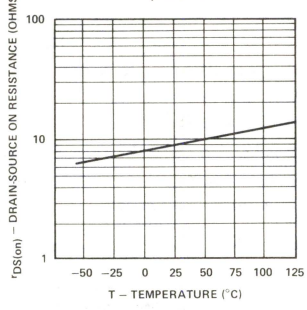
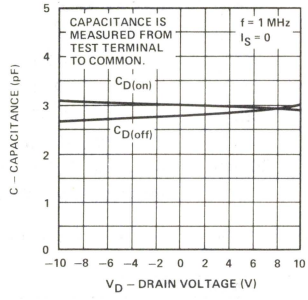
TYPICAL CHARACTERISTICS

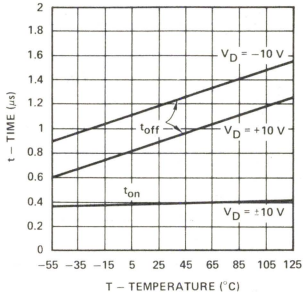
$r_{DS(on)}$ vs Temperature



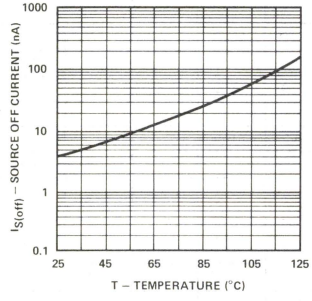
Capacitance vs V_D



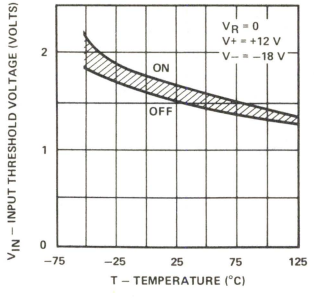
Switching Time vs V_D and Temperature



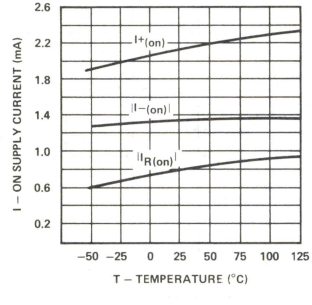
$I_{S(off)}$ vs Temperature



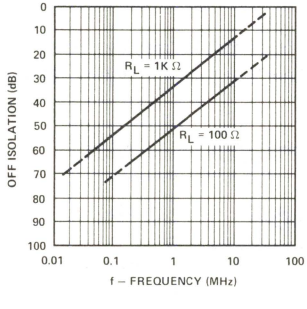
$V_{IN(th)}$ vs Temperature

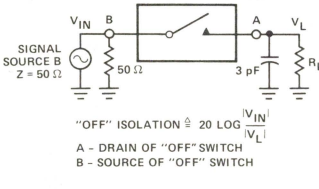


Supply Current vs Temperature

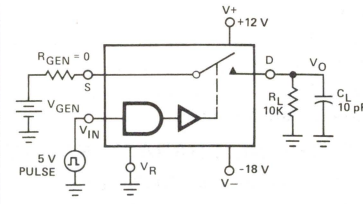


"OFF" Isolation vs R_L and Frequency

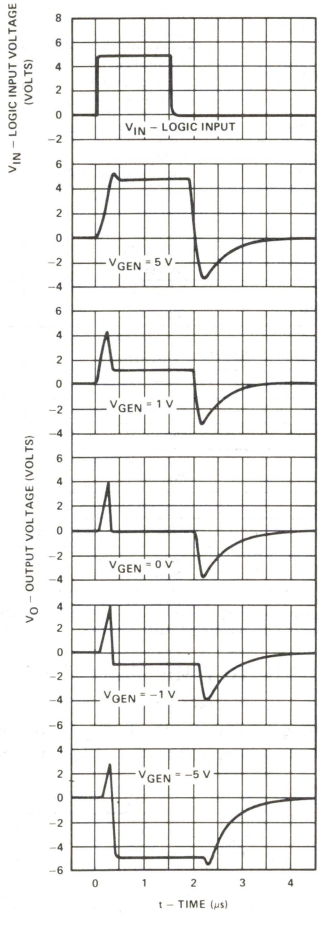




Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


V_{IN} – LOGIC INPUT VOLTAGE (VOLTS)
V_{IN} – LOGIC INPUT
V_{GEN} = 5 V
V_{GEN} = 1 V
V_{GEN} = 0 V
V_{GEN} = –1 V
V_{GEN} = –5 V
V_O – OUTPUT VOLTAGE (VOLTS)
0 1 2 3 4
t – TIME (µs)

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Drivers with Normally Open & Normally Closed Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

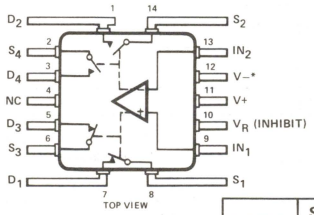
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

The DG142 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 80 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 20 V peak-to-peak. Switches have make-before-break action. The DG143 is similar to the DG142, except that it contains two FET switches instead of four. It is recommended that the DG191 and DG188 be used for new designs.

PIN CONFIGURATIONS

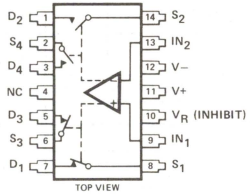
Flat Package



ORDER NUMBER:
DG142AL
SEE PACKAGE 5

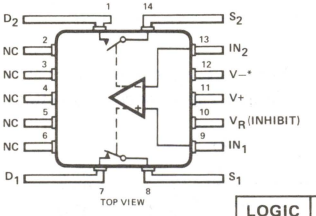
LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package



ORDER NUMBERS:
DG142AP OR DG142BP
SEE PACKAGE 11

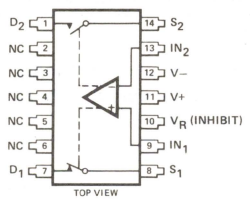
Flat Package



ORDER NUMBER:
DG143AL
SEE PACKAGE 5

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package

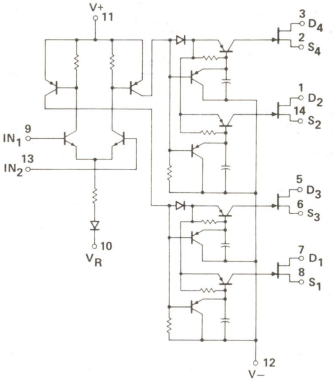


ORDER NUMBERS:
DG143AP OR DG143BP
SEE PACKAGE 11

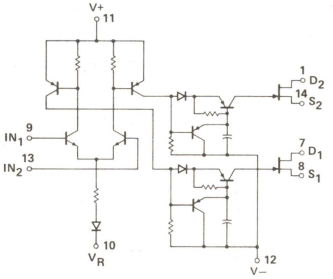
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR
V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS
(POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG142



DG143

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ABSOLUTE MAXIMUM RATINGS

V+ to V−, V_D or V_S	36 V
V_D or V_S to V−	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V
Current (Any Terminal)	30 mA

Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

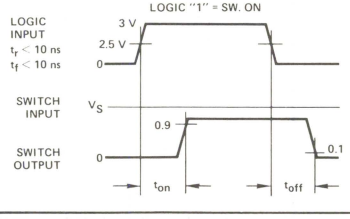
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	25°C	125°C	MAX LIMITS B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0, V_{IN2} = 2.5V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	80	80	150				Ω	V_D = 10 V	I_S = −10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							100	100	150		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 10 V, V_D = −10 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								5	100		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 10 V, V_S = −10 V	
6								5	100		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	µA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13		t_{on}	Turn-ON Time		0.8			1		µs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		1.6			2				
15	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance		**2.4 Typ			**2.4 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		**2.4 Typ			**2.4 Typ			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		**2.8 Typ			**2.8 Typ			V_D = V_S = 0	
18		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
19	SUPPLY	I+	Positive Supply Current		4.2			4.5		mA	V_{IN1} = 2 V* or V_{IN} = 3 V*, One Channel ON	
20		I−	Negative Supply Current		−2			−2.2				
21		I_R	Reference Supply Current		−2.2			−2.4				
22		I+	Positive Supply Current		25			25		µA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I−	Negative Supply Current		−25			−25				
24		I_R	Reference Supply Current		−25			−25				

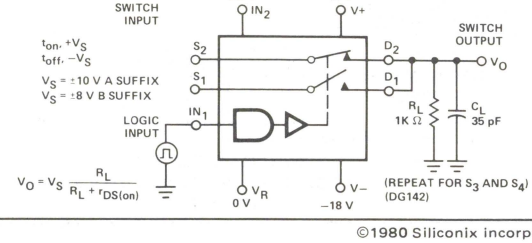
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/µs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODF + NC

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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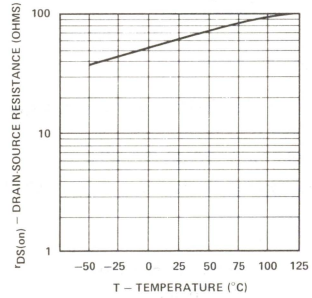
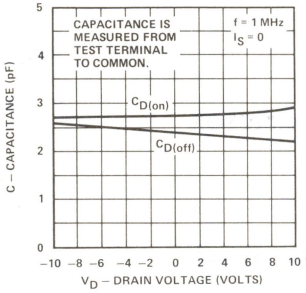
TYPICAL CHARACTERISTICS

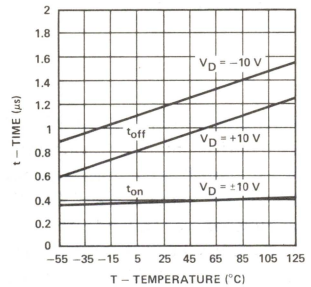
$r_{DS(on)}$ vs Temperature



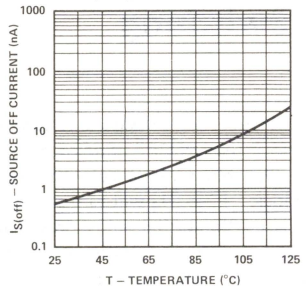
Capacitance vs V_D



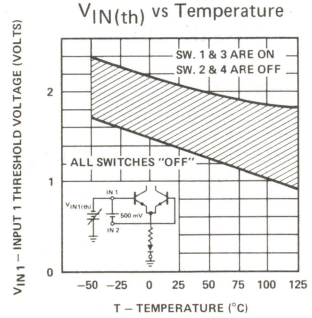
Switching Time vs V_D and Temperature



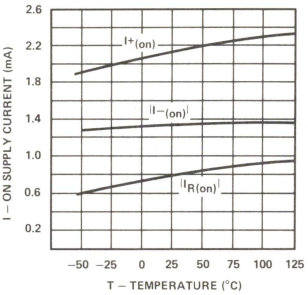
$I_{S(off)}$ vs Temperature



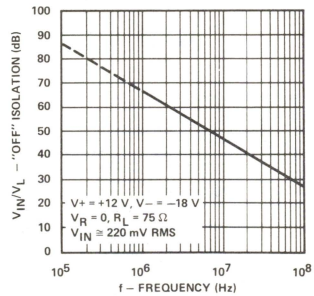
$V_{IN(th)}$ vs Temperature



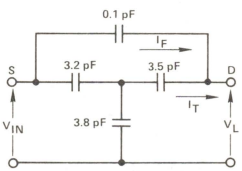
Supply Current vs Temperature



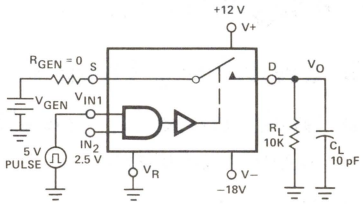
"OFF" Isolation vs R_L and Frequency



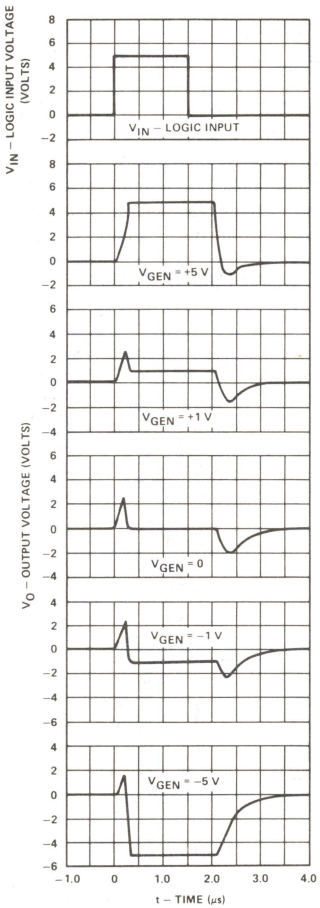
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


V_{IN} – LOGIC INPUT VOLTAGE (VOLTS)
V_{IN} – LOGIC INPUT
V_{GEN} = +5 V
V_{GEN} = +1 V
V_{GEN} = 0
V_{GEN} = –1 V
V_{GEN} = –5 V
V_O – OUTPUT VOLTAGE (VOLTS)
–1.0 0 1.0 2.0 3.0 4.0
t – TIME (μs)

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Drivers with Normally Open & Normally Closed FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

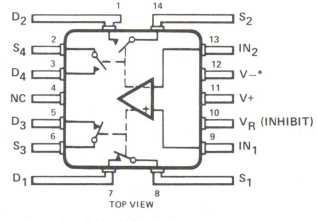
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - <1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

The DG145 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 10 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 20 V peak-to-peak. Switches have make-before-break action. The DG146 is similar to the DG145 except that it contains two FET switches instead of four. It is recommended that the DG189 and DG186 be used for new designs.

PIN CONFIGURATIONS

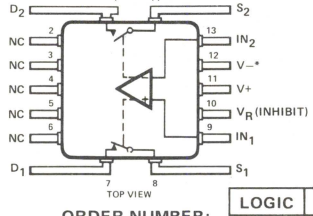
Flat Package



LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

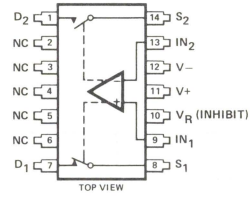
ORDER NUMBER:
DG145AL
SEE PACKAGE 5

Flat Package



ORDER NUMBER:
DG146AL
SEE PACKAGE 5

Dual-In-Line Package



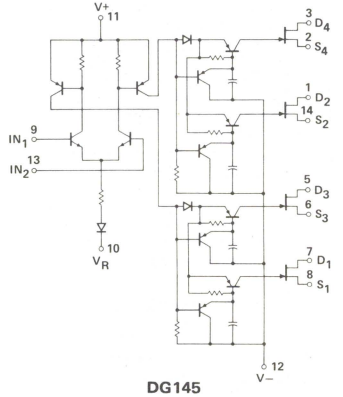
ORDER NUMBERS:
DG146AP OR DG146BP
SEE PACKAGE 11

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

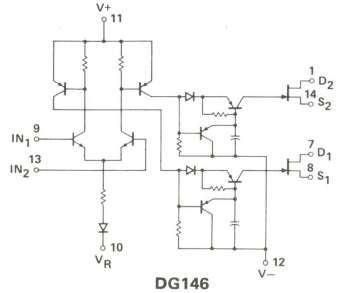
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR
V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS
(POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG145



DG146

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Siliconix

ABSOLUTE MAXIMUM RATINGS

V+ to V−, V_D or V_S	36 V
V_D or V_S to V−	32 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C

Power Dissipation*

Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.

**Derate 10 mW/°C above 75°C.

***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	25°C	125°C	B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 12 V, V− = −18 V, V_R = 0, V_{IN2} = 2.5 V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	10	10	20				Ω	V_D = 10 V	I_S = −10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							15	15	25		V_D = 8 V	
3		$I_{S(off)}$	Source OFF Leakage Current		10	1000				nA	V_S = 10 V, V_D = −10 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								15	300		V_S = 8 V, V_D = −8 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		10	1000					V_D = 10 V, V_S = −10 V	
6								15	300		V_D = 8 V, V_S = −8 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −10 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								−5	−100		V_D = V_S = −8 V	
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13	DYNAMIC	t_{on}	Turn-ON Time		1			1.5		μs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		2.5			2.5				
15		$C_{S(off)}$	Source OFF Capacitance		3 Typ**			3 Typ**		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		3 Typ**			3 Typ**			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		2.8 Typ**			2.8 Typ**			V_D = V_S = 0	
18		Off Isolation		Typ > 50 dB at f = 1 MHz**							R_L = 100 Ω, C_L = 3 pF	
19	SUPPLY	I+	Positive Supply Current		4.2			4.5		mA	V_{IN1} = 2 V* or V_{IN1} = 3 V*, One Channel ON	
20		I−	Negative Supply Current		−2			−2.2				
21		I_R	Reference Supply Current		−2.2			−2.4				
22		I+	Positive Supply Current		25			25		μA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I−	Negative Supply Current		−25			−25				
24		I_R	Reference Supply Current		−25			−25				

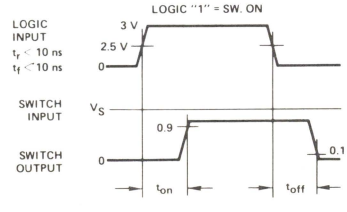
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.

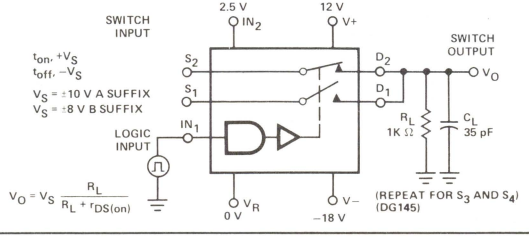
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODF + NIP

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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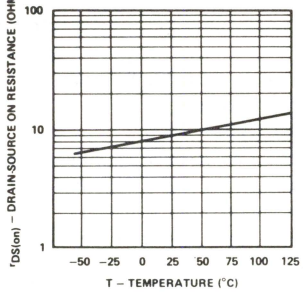
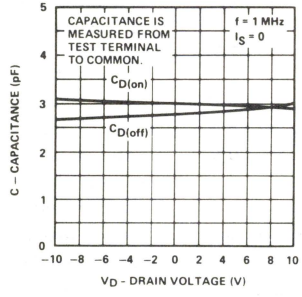
TYPICAL CHARACTERISTICS

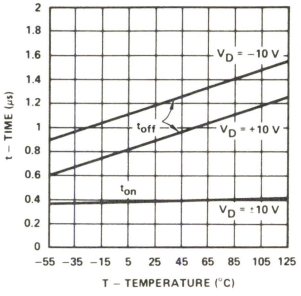
$r_{DS(on)}$ vs Temperature



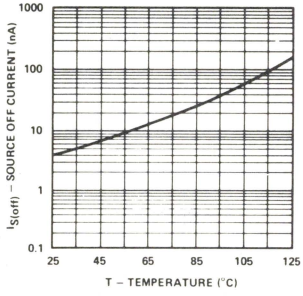
Capacitance vs V_D



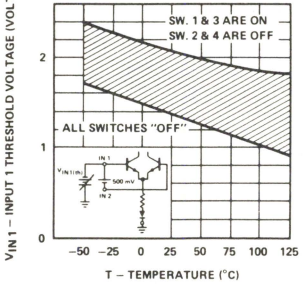
Switching Time vs V_D and Temperature



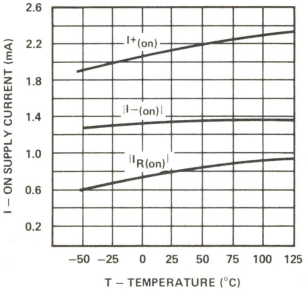
$I_{S(off)}$ vs Temperature



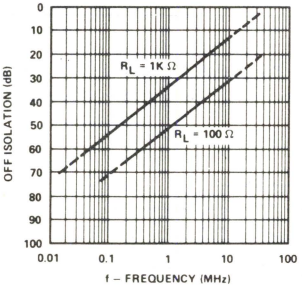
$V_{IN(th)}$ vs Temperature

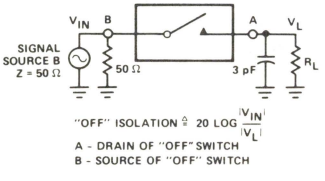


Supply Current vs Temperature

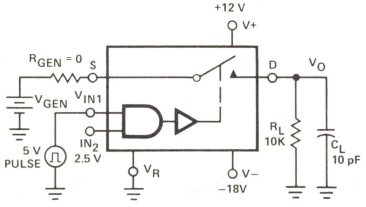


"OFF" Isolation vs R_L and Frequency

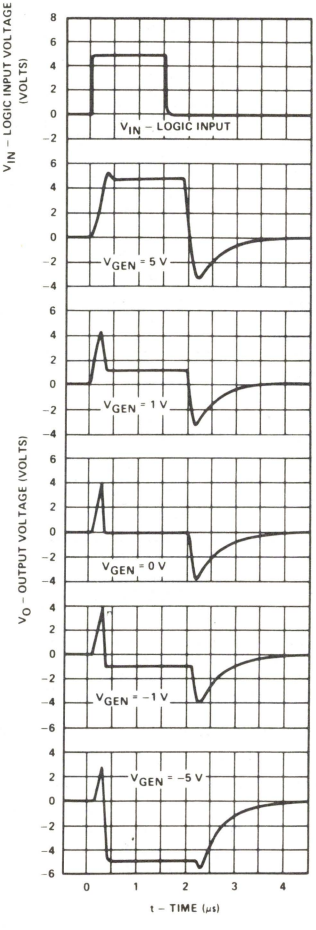




Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


VIN – LOGIC INPUT VOLTAGE (VOLTS)
VO – OUTPUT VOLTAGE (VOLTS)
VIN – LOGIC INPUT
VGEN = 5 V
VGEN = 1 V
VGEN = 0 V
VGEN = –1 V
VGEN = –5 V
0 1 2 3 4
t – TIME (µs)

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2-Channel Drivers with SPST and DPST FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

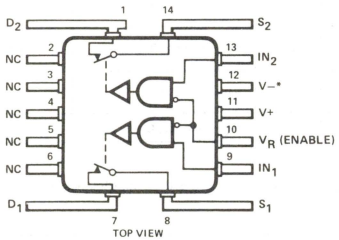
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - < 1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

The DG153 contains four junction-type field-effect transistors (JFETs) designed to function as two double-pole single-throw electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With a positive logic "0" at the driver input the switches will be OFF. With a positive logic "1" at the input the switches will be ON. In the ON state each switch will conduct current in either direction, and in the OFF state each switch will block voltages up to 15 V peak-to-peak. ON series resistance is < 15 ohms, and ON shunt leakage is < 2 nA. With both drivers in the "switch OFF" state total power consumption is < 750 μW. Switches have make-before-break action. The DG151 is similar to the DG153 except that it contains two SPST switch functions. It is recommended that the DG180 and DG183 be used for new designs.

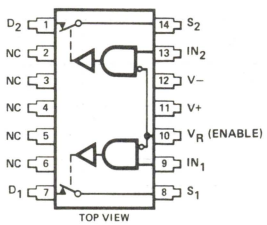
PIN CONFIGURATIONS

Flat Package



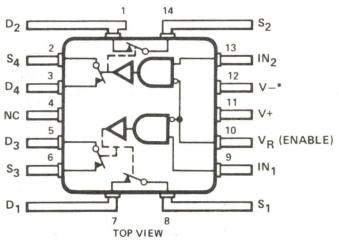
ORDER NUMBER:
DG151AL
SEE PACKAGE 5

Dual-In-Line Package



ORDER NUMBERS:
DG151AP OR DG151BP
SEE PACKAGE 11

Flat Package



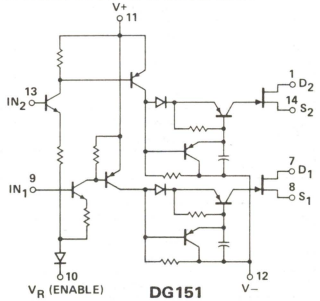
LOGIC	SWITCH
0	OFF
1	ON

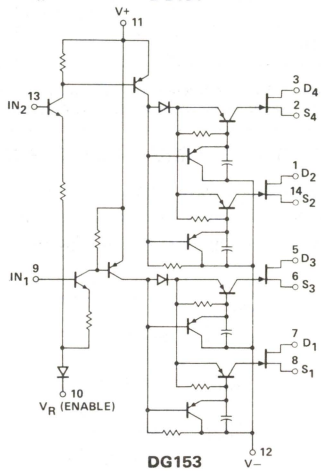
ORDER NUMBER:
DG153AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

SWITCH STATES ARE FOR LOGIC "1" INPUT

SCHEMATIC DIAGRAMS





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ABSOLUTE MAXIMUM RATINGS

V+ to V− or V_D	36 V
V_D to V−	32 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C

Power Dissipation*

Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

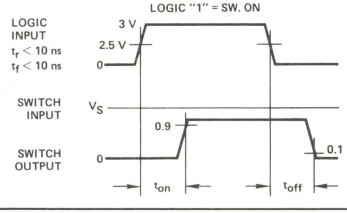
		CHARACTERISTIC		MAX LIMITS DG151A, DG153A −55°C	25°C	125°C	MAX LIMITS DG151B, DG153B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	15	15	30				Ω	V_D = 7.5 V	I_S = −10 mA, V_{IN} = 2.5 V*
2							20	20	35		V_D = 5.5 V	
3		$I_{S(off)}$	Source OFF Leakage Current		10	1000				nA	V_S = 7.5 V, V_D = −7.5 V	V_{IN} = 0.8 V*
4								15	300		V_S = 5.5 V, V_D = −5.5 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		10	1000					V_D = 7.5 V, V_S = −7.5 V	
6								15	300		V_D = 5.5 V, V_S = −5.5 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					$V_D = V_S$ = −7.5 V	V_{IN} = 2.5 V*
8								−5	−100		$V_D = V_S$ = −5.5 V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	µA	V_{IN} = 0.8 V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		V_{IN} = 2.5 V*	
11	DYNAMIC	t_{on}	Turn-ON Time		1			1.5		µs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		2.5			2.5				
13		$C_{S(off)}$	Source OFF Capacitance		** 3 Typ			** 3 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance		** 3 Typ			** 3 Typ			V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		** 2.8 Typ			** 2.8 Typ			$V_D = V_S$ = 0	
16		Off Isolation		Typ > 50 dB at 1 MHz**							R_L = 100 Ω, C_L = 3 pF	
17	SUPPLY	I+	Positive Supply Current		3			3.3		mA	V_{IN} = 2.5 V*, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		µA	V_{IN} = 0*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

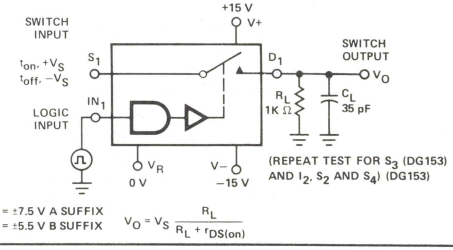
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/µs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODC + NIP

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





V_S = ±7.5 V A SUFFIX
V_S = ±5.5 V B SUFFIX

$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$

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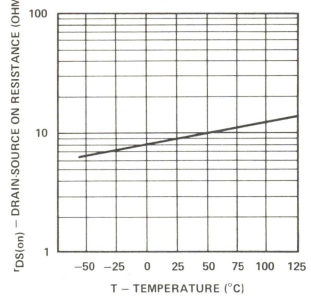
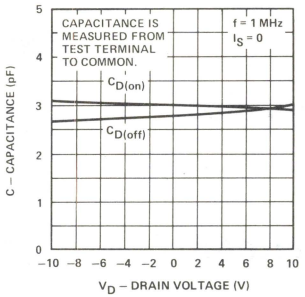
TYPICAL CHARACTERISTICS

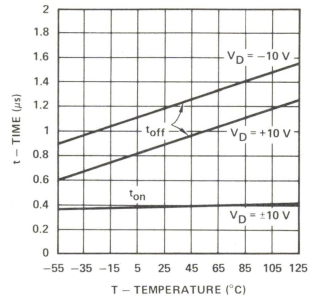
$r_{DS(on)}$ vs Temperature



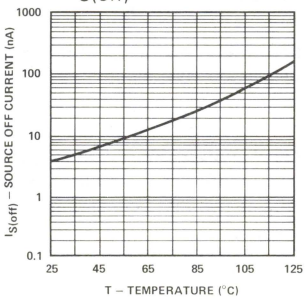
Capacitance vs V_D



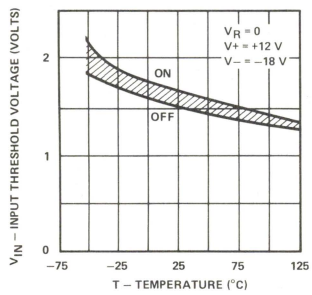
Switching Time vs V_D and Temperature



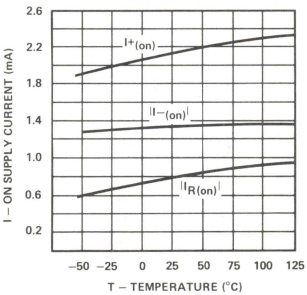
$I_{S(off)}$ vs Temperature



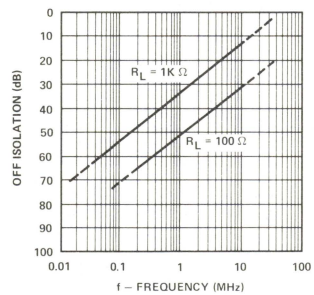
V_{IN} vs Temperature

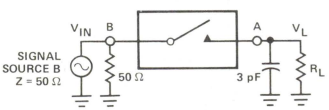


Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency

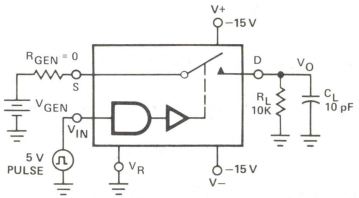




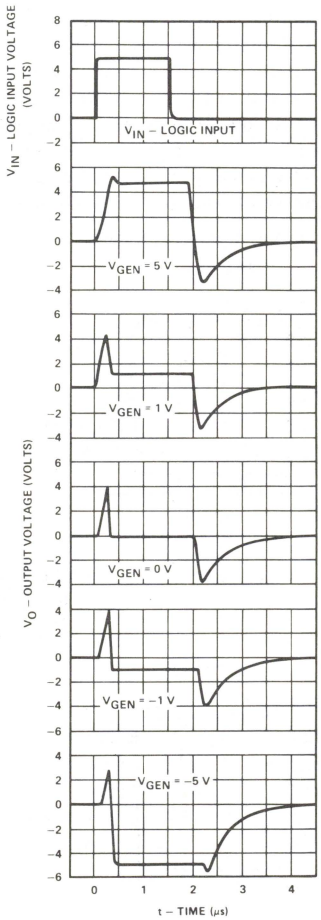
"OFF" ISOLATION ≙ 20 LOG $\frac{|V_{IN}|}{|V_L|}$

A - DRAIN OF "OFF" SWITCH
B - SOURCE OF "OFF" SWITCH

Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


VIN – LOGIC INPUT
VGEN = 5 V
VGEN = 1 V
VGEN = 0 V
VGEN = −1 V
VGEN = −5 V
VIN – LOGIC INPUT VOLTAGE (VOLTS)
VO – OUTPUT VOLTAGE (VOLTS)
0 1 2 3 4
t – TIME (µs)

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2-Channel Drivers with SPST and DPST FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

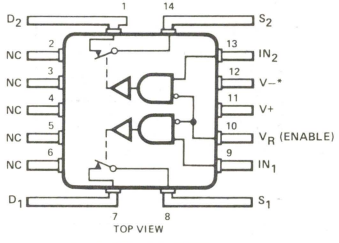
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - < 1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

The DG154 contains four junction-type field-effect transistors (JFETs) designed to function as two double-pole single-throw electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With a positive logic "0" at the driver input the switches will be OFF. With a positive logic "1" at the input the switches will be ON. In the ON state each switch will conduct current in either direction, and in the OFF state each switch will block voltages up to 15 V peak-to-peak. ON series resistance is < 50 ohms, and ON shunt leakage is < 2 nA. With both drivers in the "switch OFF" state total power consumption is < 750 μW. Switches have make-before-break action. The DG152 is similar to the DG154 except that it contains two SPST switch functions. It is recommended that the DG181 (or DG182) and DG184 (or DG185) be used for new designs.

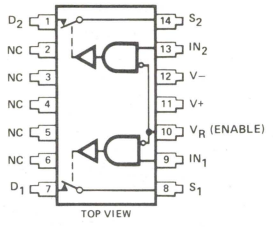
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER:
DG152AL
SEE PACKAGE 5

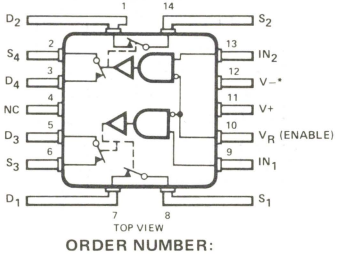
Dual-In-Line Package



ORDER NUMBERS:
DG152AP OR DG152BP
SEE PACKAGE 11

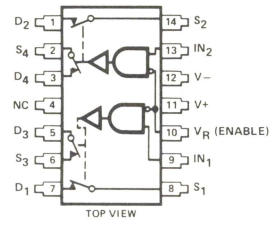
LOGIC	SWITCH
0	OFF
1	ON

Flat Package



ORDER NUMBER:
DG154AL
SEE PACKAGE 5

Dual-In-Line Package

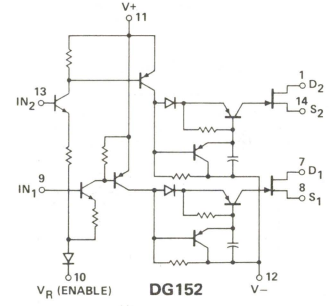


ORDER NUMBERS:
DG154AP OR DG154BP
SEE PACKAGE 11

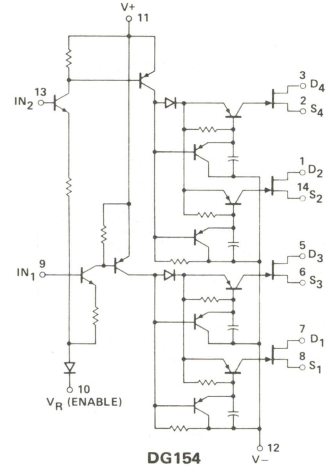
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR LOGIC "1" INPUT

SCHEMATIC DIAGRAMS



DG152



DG154

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Siliconix

ABSOLUTE MAXIMUM RATINGS

V+ to V− or V_D	36 V
V_D to V−	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V
Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

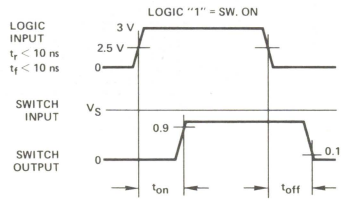
		CHARACTERISTIC		MAX LIMITS DG152A, DG154A −55°C	25°C	125°C	DG152B, DG154B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	50	50	100				Ω	V_D = 7.5 V	I_S = −10 mA, V_{IN} = 2.5 V*
2							100	100	150		V_D = 5.5 V	
3		$I_{S(off)}$	Source OFF Leakage Current		1	100				nA	V_S = 7.5 V, V_D = −7.5 V	V_{IN} = 0.8 V*
4								5	100		V_S = 5.5 V, V_D = −5.5 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		1	100					V_D = 7.5 V, V_S = −7.5 V	
6								5	100		V_D = 5.5 V, V_S = −5.5 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −7.5 V	V_{IN} = 2.5 V*
8								−5	−100		V_D = V_S = −5.5 V	
9	IN	I_{INL}	Input Current, Input Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN} = 0.8 V*	
10		I_{INH}	Input Current, Input Voltage High	120	60	60	150	100	100		V_{IN} = 2.5 V*	
11	DYNAMIC	t_{on}	Turn-ON Time		0.6			1		μs	See Switching Time Test Circuit	
12		t_{off}	Turn-OFF Time		1.6			2				
13		$C_{S(off)}$	Source OFF Capacitance		** 2.4 Typ			** 2.4 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
14		$C_{D(off)}$	Drain OFF Capacitance		** 2.4 Typ			** 2.4 Typ			V_D = 0, I_S = 0	
15		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		** 2.8 Typ			** 2.8 Typ			V_D = V_S = 0	
16		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
17	SUPPLY	I+	Positive Supply Current		3			3.3		mA	V_{IN} = 2.5 V*, One Channel ON	
18		I−	Negative Supply Current		−1.8			−2				
19		I_R	Reference Supply Current		−1.4			−1.5				
20		I+	Positive Supply Current		25			25		μA	V_{IN} = 0*, All Channels OFF	
21		I−	Negative Supply Current		−25			−25				
22		I_R	Reference Supply Current		−25			−25				

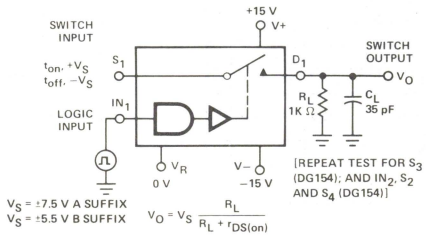
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODC + NC

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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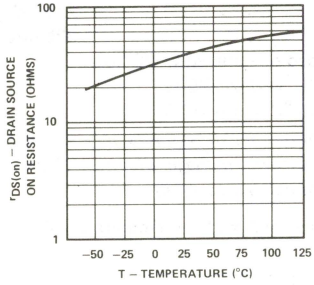
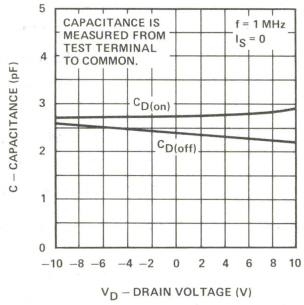
TYPICAL CHARACTERISTICS

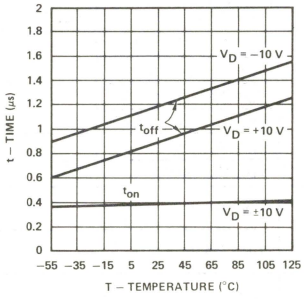
$r_{DS(on)}$ vs Temperature



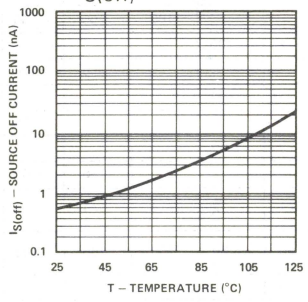
Capacitance vs V_D


CAPACITANCE IS MEASURED FROM TEST TERMINAL TO COMMON.
f = 1 MHz
I_S = 0
$C_{D(on)}$
$C_{D(off)}$
C – CAPACITANCE (pF)
–10 –8 –6 –4 –2 0 2 4 6 8 10
V_D – DRAIN VOLTAGE (V)

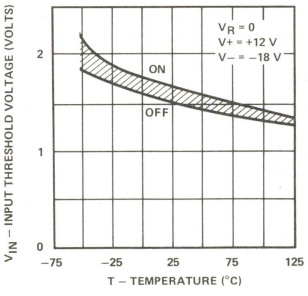
Switching Time vs V_D and Temperature



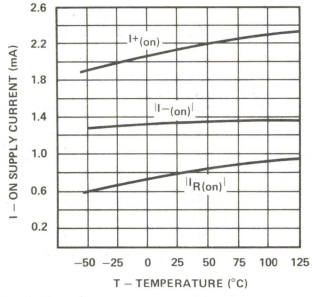
$I_{S(off)}$ vs Temperature



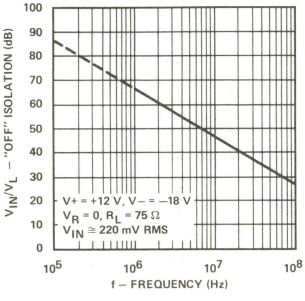
V_{IN} vs Temperature



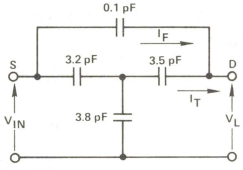
Supply Current vs Temperature



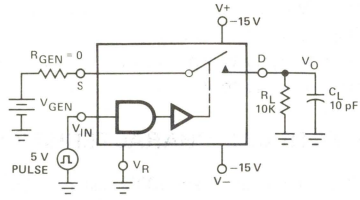
"OFF" Isolation vs R_L and Frequency



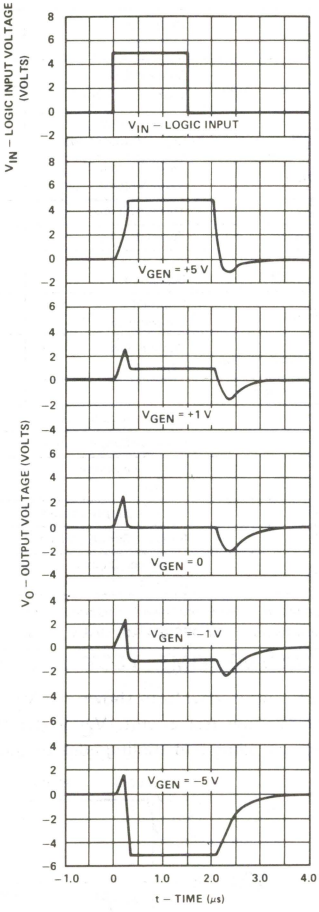
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


V_{IN} – LOGIC INPUT VOLTAGE (VOLTS)
V_{IN} – LOGIC INPUT
V_{GEN} = +5 V
V_{GEN} = +1 V
V_{GEN} = 0
V_{GEN} = –1 V
V_{GEN} = –5 V
V_O – OUTPUT VOLTAGE (VOLTS)
–1.0 0 1.0 2.0 3.0 4.0
t – TIME (µs)

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Drivers with Differentially Driven Normally Open and Normally Closed FET Switches

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

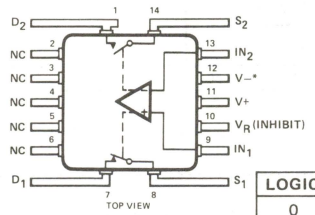
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - < 1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

The DG163 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 15 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 15 V peak-to-peak. Switches have make-before-break action. The DG161 is similar to the DG163, except that it contains two FET switches instead of four. It is recommended that the DG186 and DG189 be used for new designs.

PIN CONFIGURATIONS

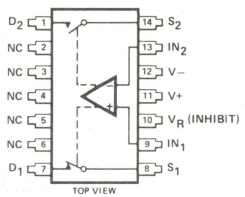
Flat Package



LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

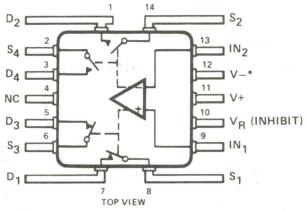
ORDER NUMBERS:
DG161AL
SEE PACKAGE 5

Dual-In-Line Package



ORDER NUMBERS:
DG161AP OR DG161BP
SEE PACKAGE 11

Flat Package



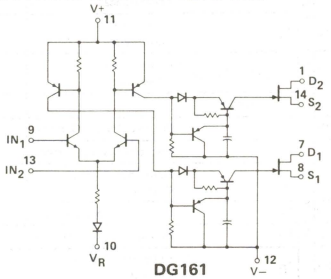
LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

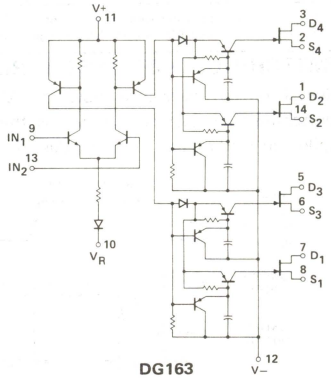
ORDER NUMBER: DG163AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

SWITCH STATES ARE FOR V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS (POSITIVE LOGIC)

SCHEMATIC DIAGRAMS





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ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D or V_S	36 V
V_D or V_S to V−	32 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

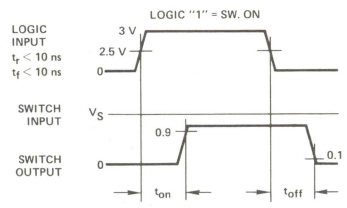
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	25°C	125°C	B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_R = 0, V_{IN2} = 2.5 V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	15	15	30				Ω	V_D = 7.5 V	I_S = −10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							20	20	35		V_D = 5.5 V	
3		$I_{S(off)}$	Source OFF Leakage Current		10	1000				nA	V_S = 7.5 V, V_D = −7.5 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								15	300		V_S = 5.5 V, V_D = −5.5 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		10	1000					V_D = 7.5 V, V_S = −7.5 V	
6								15	300		V_D = 5.5 V, V_S = −5.5 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−100					V_D = V_S = −7.5 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								−5	−100		V_D = V_S = −5.5 V	
9	IN	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13		t_{on}	Turn-ON Time		1			1.5		μs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		2.5			2.5				
15	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance		3** Typ			3** Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		3** Typ			3** Typ			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		2.8** Typ			2.8** Typ			V_D = V_S = 0	
18		Off Isolation		Typ > 50 dB at 1 MHz**							R_L = 100 Ω, C_L = 3 pF	
19	SUPPLY	I+	Positive Supply Current		4			4.4		mA	V_{IN1} = 2 V* or V_{IN1} = 3 V*, One Channel ON	
20		I−	Negative Supply Current		−2			−2.2				
21		I_R	Reference Supply Current		−2			−2.2				
22		I+	Positive Supply Current		25			25		μA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I−	Negative Supply Current		−25			−25				
24		I_R	Reference Supply Current		−25			−25				

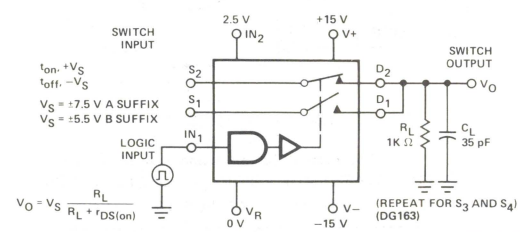
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODF + NIP

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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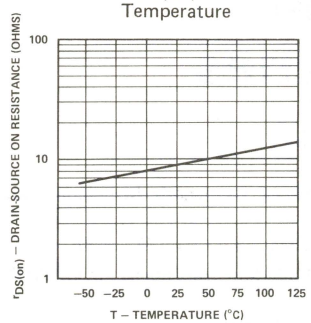
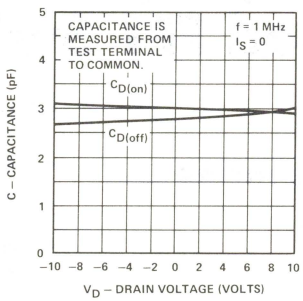
TYPICAL CHARACTERISTICS

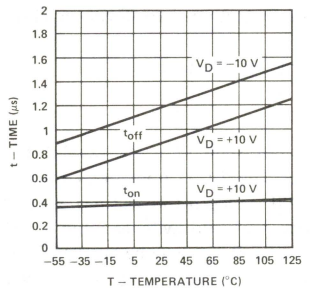
$r_{DS(on)}$ vs Temperature



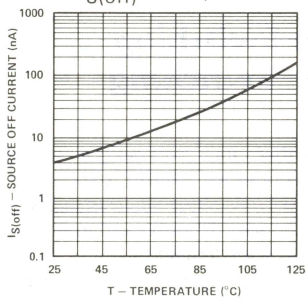
Capacitance vs V_D



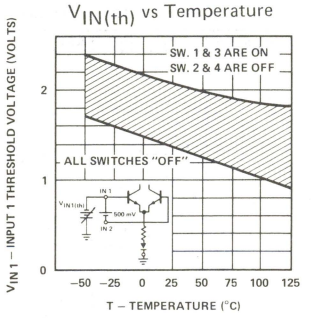
Switching Time vs V_D and Temperature



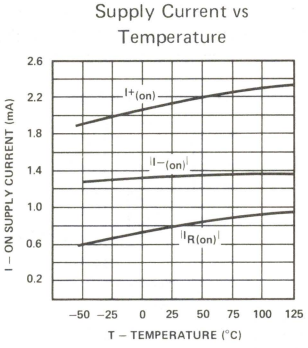
$I_{S(off)}$ vs Temperature



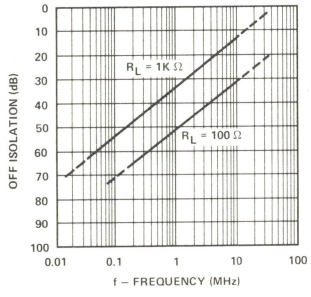
$V_{IN(th)}$ vs Temperature

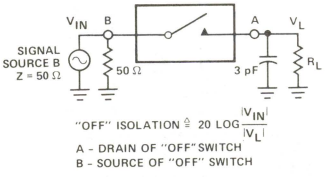


Supply Current vs Temperature

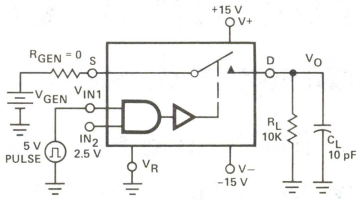


"OFF" Isolation vs R_L and Frequency

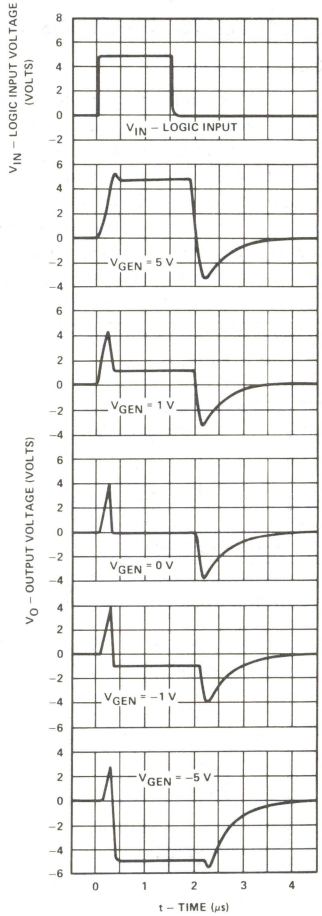




Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


V_{IN} – LOGIC INPUT VOLTAGE (VOLTS)
V_{IN} – LOGIC INPUT
V_{GEN} = 5 V
V_{GEN} = 1 V
V_{GEN} = 0 V
V_{GEN} = –1 V
V_{GEN} = –5 V
V_O – OUTPUT VOLTAGE (VOLTS)
0 1 2 3 4
t – TIME (µs)

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Drivers with Differentially Driven Normally Open and Normally Closed FET Switches

Siliconix

designed for . . .

- **Switching High Frequencies**
- **Switching in Satellite Applications**
- **Portable, Battery Operated Circuits**
- **Low Signal Distortion Switching Circuits such as Audio Switching**

BENEFITS

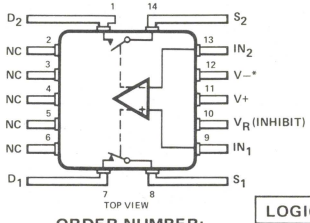
- **Higher Signal Bandwidth Switching Capabilities**
  - OFF Isolation > 60 dB @ 1 MHz
- **Better Radiation Resistance than PMOS Drivers**
  - Bipolar Drivers
- **Minimizes Standby Power Requirements**
  - < 1 mW Standby Power
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance

DESCRIPTION

The DG164 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R. In the ON state, each switch conducts equally well in either direction, has a series resistance of < 50 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 15 V peak-to-peak. Switches have make-before-break action. The DG162 is similar to the DG164, except that it contains two FET switches instead of four. It is recommended that the DG187 (or DG188) and DG190 (or DG191) be used for new designs.

PIN CONFIGURATIONS

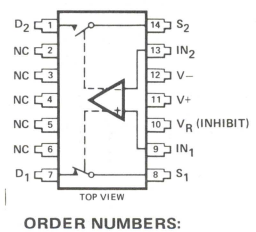
Flat Package



ORDER NUMBER:
DG162AL
SEE PACKAGE 5

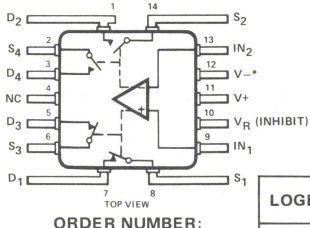
LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

Dual-In-Line Package



ORDER NUMBERS:
DG162AP OR DG162BP
SEE PACKAGE 11

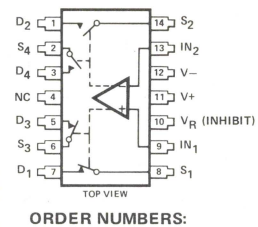
Flat Package



ORDER NUMBER:
DG164AL
SEE PACKAGE 5

LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package

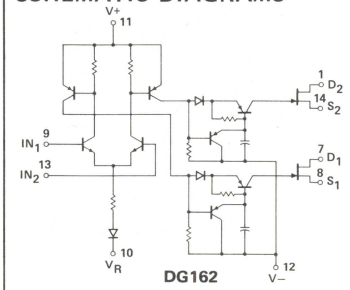


ORDER NUMBERS:
DG164AP OR DG164BP
SEE PACKAGE 11

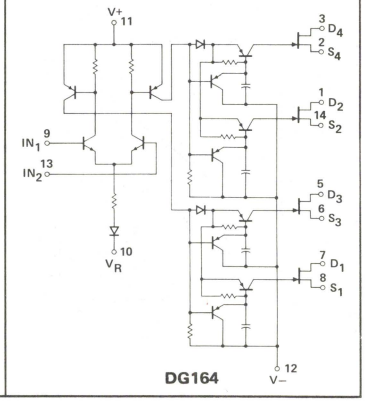
*Common to Substrate and Base of Package

SWITCH STATES ARE FOR V_{IN1} = LOGIC "1" INPUT AND V_{IN2} = 2.5 V BIAS (POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



DG162



DG164

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ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D or V_S	36 V
V_D or V_S to V−	36 V
V_D to V_S	±22 V
V+ to V_R	25 V
V+ to V_{IN1} or V_{IN2}	25 V
V_R to V−	25 V
V_{IN1} to V_{IN2}	±6 V
V_{IN1} or V_{IN2} to V_R	±6 V
V_{IN1} or V_{IN2} to V−	30 V

Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C

Power Dissipation*

Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

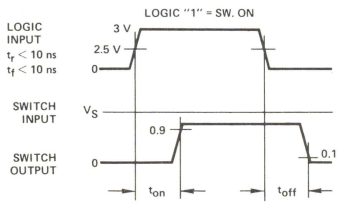
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX −20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_R = 0, V_{IN2} = 2.5 V*	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	50	50	100				Ω	V_D = 7.5 V	I_S = −10 mA, V_{IN1} = 3 V* ($SW_{1,3}$ ON), V_{IN1} = 2 V* ($SW_{2,4}$ ON)
2							100	100	150		V_D = 5.5 V	
3		$I_{S(off)}$	Source OFF Leakage Current		2	100				nA	V_S = 7.5 V, V_D = −7.5 V	V_{IN1} = 2 V* ($SW_{1,3}$ OFF), V_{IN1} = 3 V* ($SW_{2,4}$ OFF)
4								5	100		V_S = 5.5 V, V_D = −5.5 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		2	100					V_D = 7.5 V, V_S = −7.5 V	
6								5	100		V_D = 5.5 V, V_S = −5.5 V	
7		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	100					V_D = V_S = −7.5 V	V_{IN1} = 3 V* ($SW_{1,3}$ ON) V_{IN1} = 2 V* ($SW_{2,4}$ ON)
8								−5	100		V_D = V_S = −5.5 V	
9	INPUT	I_{IN1L}	Input 1 Current, Input 1 Voltage Low	0.1	0.1	2	4	4	4	μA	V_{IN1} = 2 V*	
10		I_{IN2L}	Input 2 Current, Input 2 Voltage Low	0.1	0.1	2	4	4	4		V_{IN2} = 2 V*, V_{IN1} = 2.5 V*	
11		I_{IN1H}	Input 1 Current, Input 1 Voltage High	120	60	60	150	100	100		V_{IN1} = 3 V*	
12		I_{IN2H}	Input 2 Current, Input 2 Voltage High	120	60	60	150	100	100		V_{IN2} = 3 V*, V_{IN1} = 2.5 V*	
13	DYNAMIC	t_{on}	Turn-ON Time		0.8			1		μs	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time		1.6			2				
15		$C_{S(off)}$	Source OFF Capacitance		** 2.4 Typ			** 2.4 Typ		pF	V_S = 0, I_D = 0	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance		** 2.4 Typ			** 2.4 Typ			V_D = 0, I_S = 0	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		** 2.8 Typ			** 2.8 Typ			V_D = V_S = 0	
18		Off Isolation		Typ > 60 dB at 1 MHz**							R_L = 75 Ω	
19	SUPPLY	I+	Positive Supply Current		4			4.4		mA	V_{IN1} = 2 V* or V_{IN1} = 3 V*, One Channel ON	
20		I−	Negative Supply Current		−2			−2.2				
21		I_R	Reference Supply Current		−2			−2.2				
22		I+	Positive Supply Current		25			25		μA	V_{IN1} = V_{IN2} = 0.8 V*, All Channels OFF	
23		I−	Negative Supply Current		−25			−25				
24		I_R	Reference Supply Current		−25			−25				

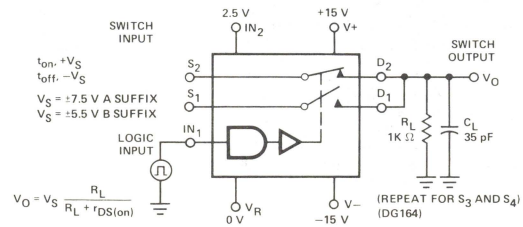
*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

LODF + NC

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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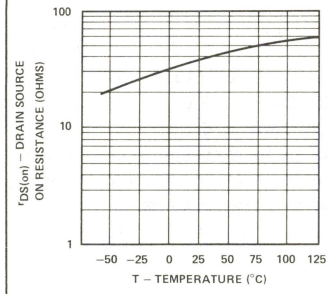
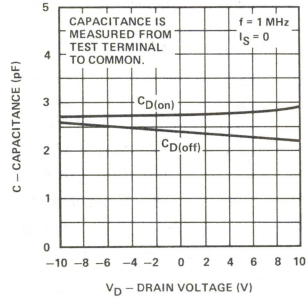
TYPICAL CHARACTERISTICS

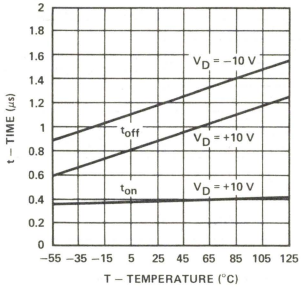
$r_{DS(on)}$ vs Temperature



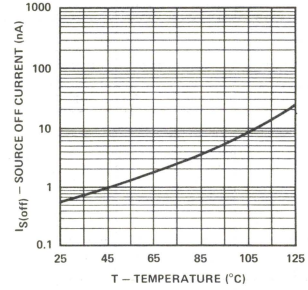
Capacitance vs V_D



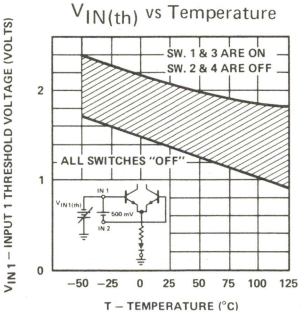
Switching Time vs V_D and Temperature



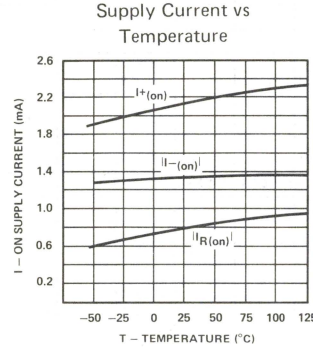
$I_{S(off)}$ vs Temperature



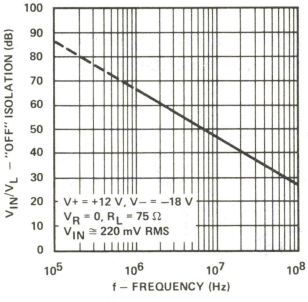
$V_{IN(th)}$ vs Temperature



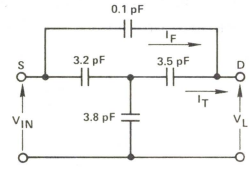
Supply Current vs Temperature



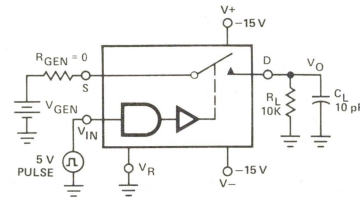
"OFF" Isolation vs R_L and Frequency



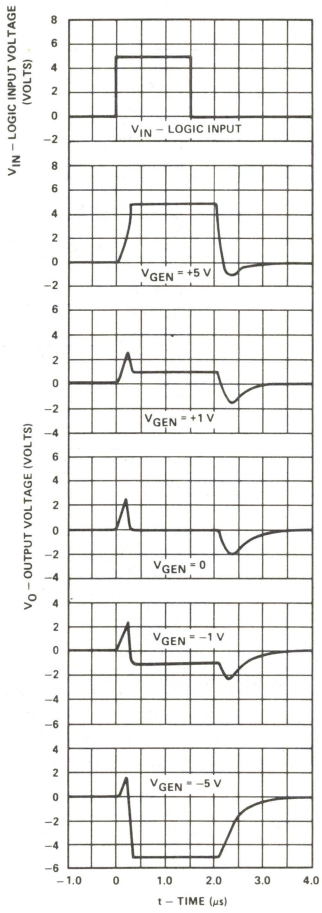
Equivalent "OFF" Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.


V_{IN} – LOGIC INPUT VOLTAGE (VOLTS)
V_{IN} – LOGIC INPUT
V_{GEN} = +5 V
V_{GEN} = +1 V
V_{GEN} = 0
V_{GEN} = –1 V
V_{GEN} = –5 V
V_O – OUTPUT VOLTAGE (VOLTS)
–1.0 0 1.0 2.0 3.0 4.0
t – TIME (μs)

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Monolithic 4-Channel Driver with PMOS Switches

Siliconix

designed for . . .

- **Make-Before-Break Switching i.e. Feedback Resistor Switching in Variable Gain Op-Amps**
- **Low Leakage Switching such as Sample and Hold Circuits**

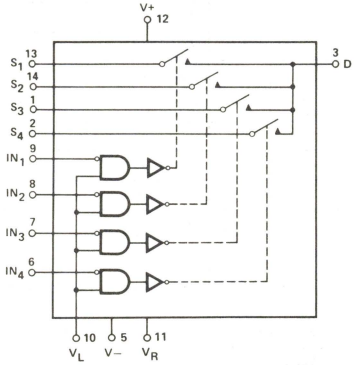
BENEFITS

- **Easily Interfaced**
  - TTL, CMOS, DTL Direct Drive Compatibility
- **Reduces External Component Requirements**
  - No Interface Components Required
  - Voltage–Limiting Diodes Protect PMOS Gates

DESCRIPTION

The DG172 contains four MOS field-effect transistors designed to function as electronic switches. Level-shifting drivers enable a low-level input (0.8 to 2.0 V) to control the ON-OFF condition of each switch. In the ON state, each switch will conduct current equally well in either direction. In the OFF state, the switches will block voltages up to 20 V peak-to-peak. Positive logic "0" at the driver input will turn each switch ON. A common driver terminal V_L may be used to clock all four switches by switching the device from the ENABLE mode ($\geqslant$ 4 V) to the INHIBIT mode ($\leqslant$ 0.4 V).

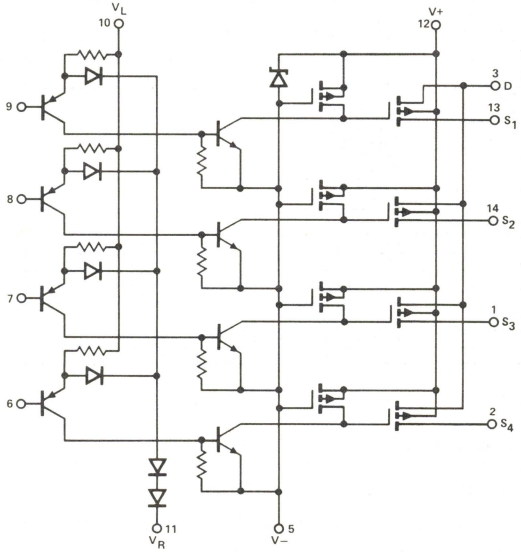
FUNCTIONAL DIAGRAM



LOGIC	SWITCH
0	ON
1	OFF

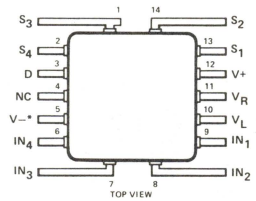
SWITCH STATES ARE FOR LOGIC "1" INPUT.
(POSITIVE LOGIC)

SCHEMATIC DIAGRAM



PIN CONFIGURATIONS

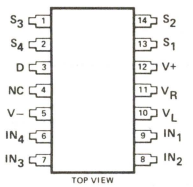
Flat Package



ORDER NUMBER: DG172AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

Dual-In-Line Package



ORDER NUMBERS: DG172AP OR DG172BP
SEE PACKAGE 11

DG172CJ
SEE PACKAGE 7

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ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	25 V
V+ to V_S	25 V
V_S to V−	36 V
V_D to V−	36 V
V_S to V_D	25 V
V_L to V−	30 V
V_L to V_{IN}	±6 V
V_L to V_R	±6 V
V_{IN} to V_R	±6 V
Current (Any Terminal)	20 mA
Storage Temperature (A & B Suffix)	−65 to 150°C
(C Suffix)	-65 to 125°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
(C Suffix)	0 to 70°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP (ceramic)***	825 mW
14 Pin Plastic DIP****	470 mW

*All leads welded or soldered to PC board

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

****Derate 6.3 mW/°C above 25°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

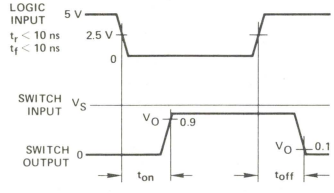
		CHARACTERISTIC		MAX LIMITS DG172A −55°C	DG172A 25°C	DG172A 125°C	DG172B −20°C	DG172B 25°C	DG172B 85°C	DG172C 25°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_L = 5 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	250	150	150	200	200	Ω	V_D = 10 V	I_S = −1 mA, V_{IN} = 0.8 V
2				200	200	350	225	225	300	300		V_D = 0	
3				450	450	600	500	500	600	600		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		−1	−1000		−5	−100	−10	nA	V_S = −10 V, V_D = 10 V	V_{IN} = 2 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−4	−4000		−10	−300	−10		V_D = −10 V, V_S = 10 V	
6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		4	4000		10	300	10		$V_D = V_S$ = 10 V	V_{IN} = 0.8 V
7	IN	I_{INL}	Input Current, Input Voltage Low	−0.5	−0.5	−0.5	−1	−1	−1	−1	mA	V_{IN} = 0	
8		I_{INH}	Input Current, Input Voltage High	0.1	0.1	10	0.1	1	10	1	μA	V_{IN} = 5 V	
9	DYNAMIC	t_{on}	Turn-ON Time		0.3			0.5		0.08 Typ*	μs	See Switching Time Test Circuit	
10		t_{off}	Turn-OFF Time		0.75			1		0.5 Typ*			
11		$C_{S(off)}$	Source OFF Capacitance	5 Typical*							pF	V_S = 0, I_D = 0	f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance	18 Typical*								V_D = 0, I_S = 0	
13		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	28 Typical*								$V_D = V_S$ = 0	
14		Off Isolation		Typ > 50 dB at 5 MHz*								R_L = 100 Ω, C_L = 3 pF	
15	SUPPLY	I+	Positive Supply Current		3			3		3	mA	V_{IN} = 0, One Channel ON; I_R = 0	
16		I−	Negative Supply Current		−5.1			−5.1		−5.1			
17		I_L	Logic Supply Current		5.7			5.7		5.7			
18					2.1			2.1		2.1			
19		I_R	Reference Supply Current		−3.6			−3.6		−3.6			
20		I+	Positive Supply Current		10			10		10	μA	V_{IN} = 5 V, All Channels OFF; I_R = 0	
21		I−	Negative Supply Current		−20			−20		−20			
22		I_L	Logic Supply Current		4.5			4.5		4.5	mA		
23					10			10		10	μA		
24		I_R	Reference Supply Current		−4.5			−4.5		−4.5	mA		

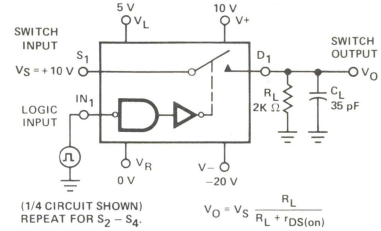
*Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing

CMD

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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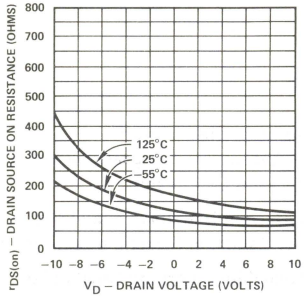
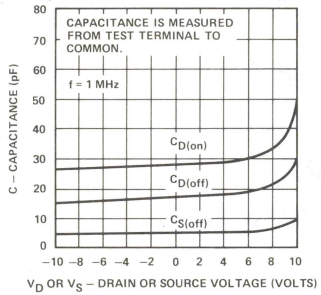
TYPICAL CHARACTERISTICS

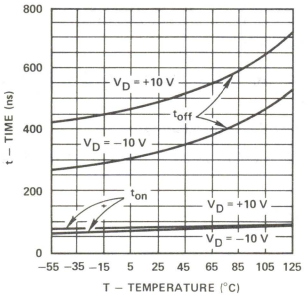
$r_{DS(on)}$ vs V_D and Temperature



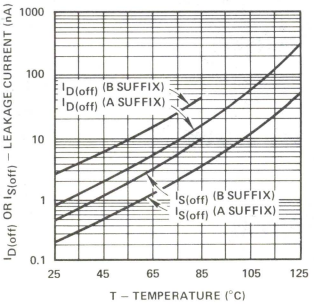
Capacitance vs V_D or V_S



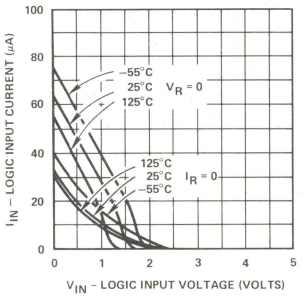
Switching Time vs V_D and Temperature



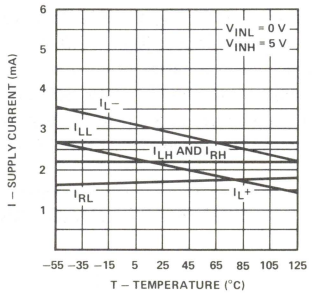
$I_{D(off)}/I_{S(off)}$ vs Temperature



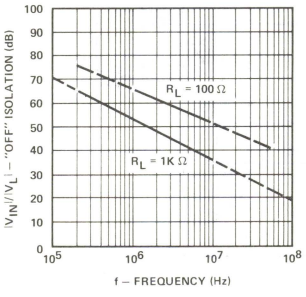
I_{IN} vs V_{IN} and Temperature

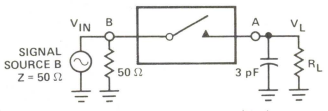


Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency

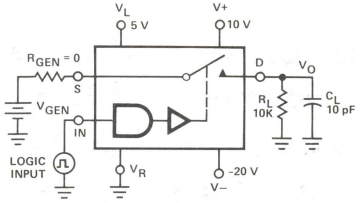




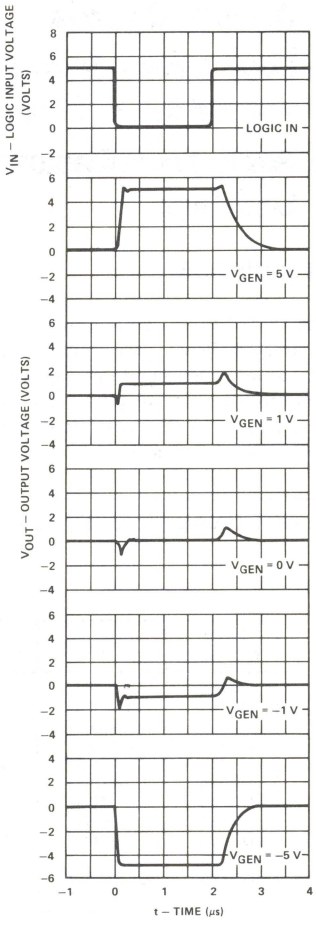
"OFF" ISOLATION ≙ 20 LOG $\frac{|V_{IN}|}{|V_L|}$

A – DRAIN OF "OFF" SWITCH
B – SOURCE OF "OFF" SWITCH

Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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High-Speed Driver with JFET Switches *designed for...*

Siliconix

- **Fast Acquisition Speed in Sample and Hold Circuits**
- **Low Leakage Switching Applications i.e. Sample and Hold Circuits**
- **High Frequency Signal Switching such as Video Signals**
- **Low Distortion Switching, Audio Signals**
- **Low Level Switching in Low Impedance Circuits**
- **Fast, Low Resistance D/A Ladders**

JAN QUALIFIED

BENEFITS

- **Eliminates Large Signal Error**
  - < 2 nA Leakage from Signal Channel in Both ON and OFF States
- **Increased Current Handling Capabilities**
  - 200 mA Maximum Switching Current
- **Higher Bandwidth Switching Capabilities**
  - Cross-Talk and OFF Isolation > 55 dB at 1 MHz (75 Ω Load)
- **Easily Interfaced**
  - TTL, DTL, RTL Direct Drive Compatibility
- **Less Signal Distortion than CMOS or PMOS Switches**
  - Constant ON Resistance
- **Low Voltage Drop Across Switch in the ON State**
  - $r_{ds(on)} \leq 10\ \Omega$

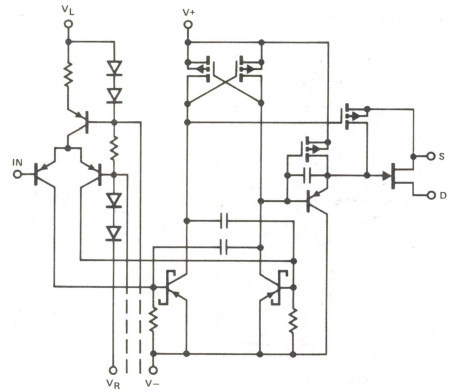
DESCRIPTION

The DG180 series contains two to four N-channel junction-type field-effect transistors (JFET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.0 V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block voltages up to 20 V peak-to-peak. Switch-OFF input-output feed-through is > 60 dB at 10 MHz, because of the low output impedance of the FET-gate driving circuit.

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	R_{ON} (MAX)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75

SCHEMATIC DIAGRAM (Typical Channel)



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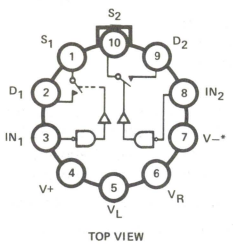
PIN CONFIGURATIONS

DUAL SPST

LOGIC	SWITCH
0	ON
1	OFF

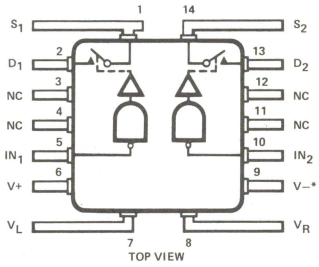
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Metal Can Package



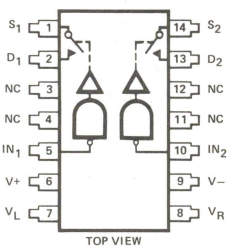
ORDER NUMBERS:
DG180AA OR DG180BA
DG181AA OR DG181BA
DG182AA OR DG182BA
SEE PACKAGE 2
*Common to Substrate and Case

Flat Package



ORDER NUMBER:
DG181AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



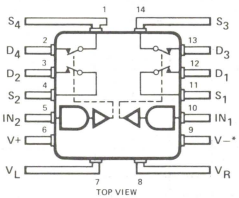
ORDER NUMBERS:
DG180AP OR DG180BP
DG181AP OR DG181BP
DG182AP OR DG182BP
SEE PACKAGE 11

DUAL DPST

LOGIC	SWITCH
0	OFF
1	ON

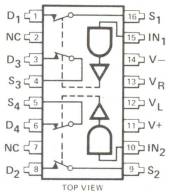
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Flat Package



ORDER NUMBERS:
DG184AL OR DG185AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



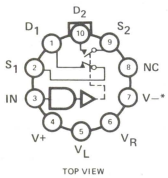
ORDER NUMBERS:
DG183AP OR DG183BP
DG184AP OR DG184BP
DG185AP OR DG185BP
SEE PACKAGE 12

SPDT

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

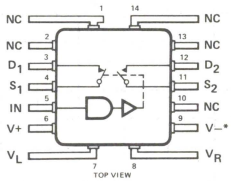
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Metal Can Package



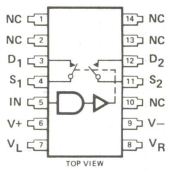
ORDER NUMBERS:
DG186AA OR DG186BA
DG187AA OR DG187BA
DG188AA OR DG188BA
SEE PACKAGE 2
*Common to Substrate and Case

Flat Package



ORDER NUMBERS:
DG187AL OR DG188AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



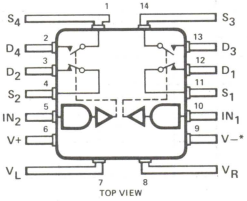
ORDER NUMBERS:
DG186AP OR DG186BP
DG187AP OR DG187BP
DG188AP OR DG188BP
SEE PACKAGE 11

DUAL SPDT

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

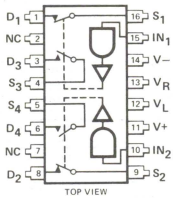
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Flat Package



ORDER NUMBERS:
DG190AL OR DG191AL
SEE PACKAGE 5
*Common to Substrate and Base of Package

Dual-In-Line Package



ORDER NUMBERS:
DG189AP OR DG189BP
DG190AP OR DG190BP
DG191AP OR DG191BP
SEE PACKAGE 12

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ABSOLUTE MAXIMUM RATINGS

V+ to V–	36 V
V+ to V_D	33 V
V_D to V–	30 V
V_D to V_S	±22 V
V_L to V–	36 V
V_L to V_{IN}	8 V
V_L to V_R	8 V
V_{IN} to V_R	8 V
V_R to V–	27 V
V_R to V_{IN}	2 V
Current (Any Terminal except S or D)	30 mA
Currents (S or D) 30 Ω, 75 Ω	30 mA
10 Ω Only	200 mA
Storage Temperature	–65 to 150°C
Operating Temperature (A Suffix)	–55 to 125°C
(B Suffix)	–20 to 85°C

Power Dissipation*

Metal Can**	450 mW
14 Pin DIP***	825 mW
16 Pin DIP****	900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.
****Derate 12 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

			CHARACTERISTIC		MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX –20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = –15 V, V_L = 5 V, V_R = 0	
10 Ω	DG180, DG183, DG186, DG189	1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	10	10	20	10	10	20	Ω	V_D = –7.5 V	I_S = –10 mA, V_{IN} = 0.8 V or 2.0 V, Note 1
		2		$I_{S(off)}$	Source OFF Leakage Current		10	1000		15	300	nA	V_S = 10 V, V_D = –10 V; V+ = 10 V, V– = –20 V	V_{IN} = 2.0 V or 0.8 V, Note 2
		3					10	1000		15	300		V_S = 7.5 V, V_D = –7.5 V	
		4		$I_{D(off)}$	Drain OFF Leakage Current		10	1000		15	300		V_D = 10 V, V_S = –10 V; V+ = 10 V, V– = –20 V	
		5					10	1000		15	300		V_D = 7.5 V, V_S = –7.5 V	
		6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		–2	–200		–10	–200		V_D = V_S = –7.5 V	
		7		I_{DSS}	Saturation Drain Current	300 Typical*						mA	2 msec Pulse Duration	
		8	IN	I_{INL}	Input Current, Input Voltage Low	–250	–250	–250	–250	–250	–250	µA	V_{IN} = 0	
		9		I_{INH}	Input Current, Input Voltage High		10	20		10	20		V_{IN} = 5 V	
		10	DYNAMIC	t_{on}	Turn-ON Time		300			350		ns	See Switching Time Test Circuit	
		11		t_{off}	Turn-OFF Time		250			300				
		12		$C_{S(off)}$	Source OFF Capacitance	21 Typical*						pF	V_S = –5 V, I_D = 0	f = 1 MHz
		13		$C_{D(off)}$	Drain OFF Capacitance	17 Typical*							V_D = 5 V, I_S = 0	
		14		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	17 Typical*							V_D = V_S = 0	
		15			OFF Isolation	Typical > 55 dB at 1 MHz *							R_L = 75 Ω	
30 Ω	DG181, DG184, DG187, DG190	1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	30	30	60	50	50	75	Ω	V_D = –7.5 V	I_S = –10 mA, V_{IN} = 0.8 V or 2.0 V, Note 1
		2		$I_{S(off)}$	Source OFF Leakage Current		1	100		5	100	nA	V_S = 10 V, V_D = –10 V; V+ = 10 V, V– = –20 V	V_{IN} = 2.0 V or 0.8 V, Note 2
		3					1	100		5	100		V_S = 7.5 V, V_D = –7.5 V	
		4		$I_{D(off)}$	Drain OFF Leakage Current		1	100		5	100		V_D = 10 V, V_S = –10 V; V+ = 10 V, V– = –20 V	
		5					1	100		5	100		V_D = 7.5 V, V_S = –7.5 V	
		6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		–2	–200		–10	–200		V_D = V_S = –7.5 V	
		7	IN	I_{INL}	Input Current, Input Voltage Low	–250	–250	–250	–250	–250	–250	µA	V_{IN} = 0	
		8		I_{INH}	Input Current, Input Voltage High		10	20		10	20		V_{IN} = 5 V	
		9	DYNAMIC	t_{on}	Turn-ON Time		150			180		ns	See Switching Time Test Circuit	
		10		t_{off}	Turn-OFF Time		130			150				
		11		$C_{S(off)}$	Source OFF Capacitance	9 Typical*						pF	V_S = –5 V, I_D = 0	f = 1 MHz
		12		$C_{D(off)}$	Drain OFF Capacitance	6 Typical*							V_D = –5 V, I_S = 0	
		13		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	14 Typical*							V_D = V_S = 0	
		14			Off Isolation	Typical > 50 dB at 10 MHz							R_L = 75 Ω	
75 Ω	DG182, DG185, DG188, DG191	1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	75	75	100	100	100	150	Ω	V_D = –10 V	I_S = –10 mA, V_{IN} = 0.8 V or 2.0 V, Note 1
		2		$I_{S(off)}$	Source OFF Leakage Current		1	100		5	100	nA	V_S = 10 V, V_D = –10 V; V+ = 10 V, V– = –20 V	V_{IN} = 2.0 V or 0.8 V, Note 2
		3					1	100		5	100		V_S = 10 V, V_D = –10 V	
		4		$I_{D(off)}$	Drain OFF Leakage Current		1	100		5	100		V_D = 10 V, V_S = –10 V; V+ = 10 V, V– = –20 V	
		5					1	100		5	100		V_D = 10 V, V_S = –10 V	
		6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		–2	–200		–10	–200		V_D = V_S = –10 V	
		7	IN	I_{INL}	Input Current, Input Voltage Low	–250	–250	–250	–250	–250	–250	µA	V_{IN} = 0	
		8		I_{INH}	Input Current, Input Voltage High		10	20		10	20		V_{IN} = 5 V	
		9	DYNAMIC	t_{on}	Turn-ON Time		250			300		ns	See Switching Time Test Circuit	
		10		t_{off}	Turn-OFF Time		130			150				
		11		$C_{S(off)}$	Source OFF Capacitance	9 Typical*						pF	V_S = –5 V, I_D = 0	f = 1 MHz
		12		$C_{D(off)}$	Drain OFF Capacitance	6 Typical*							V_D = –5 V, I_S = 0	
		13		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	14 Typical*							V_D = V_S = 0	
		14			Off Isolation	Typical > 50 dB at 10 MHz							R_L = 75 Ω	

NOTES: 1. V_{IN} = 0.8 V or 2.0 V to turn ON switch under test. 2. V_{IN} = 0.8 V or 2.0 V to turn OFF switch under test.

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ELECTRICAL CHARACTERISTICS Power Supply Current (25°C)

CHARACTERISTIC		A OR B SUFFIX MAX LIMITS DG180, DG181 DG183, DG187 DG190, DG191	DG183 DG184 DG185	DG186 DG187 DG188	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_L = 5 V, V_R = 0
I+	Positive Supply Current	1.5	3	0.8	mA	All V_{IN} = 0 V
I−	Negative Supply Current	−5	−5.5	−3		
I_L	Logic Supply Current	4.5	4.5	3.2		
I_R	Reference Supply Current	−2	−2	−2		
I+	Positive Supply Current	1.5	0.1	0.8		All V_{IN} = 5 V
I−	Negative Supply Current	−5	−4	−3		
I_L	Logic Supply Current	4.5	4.5	3.2		
I_R	Reference Supply Current	−2	−2	−2		

CMJA + NC – DG184,DG185
CMJA + NIP – DG183

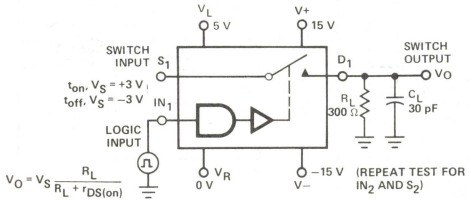
CMJB + NC – DG181, DG182, DG190, DG191
CMJB + NIP – DG180, DG189

CMJC + NC – DG187, DG188
CMJC + NIP – DG186

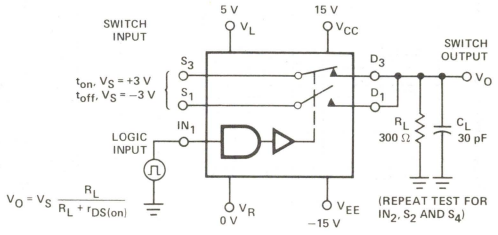
SWITCHING TIME TEST CIRCUITS

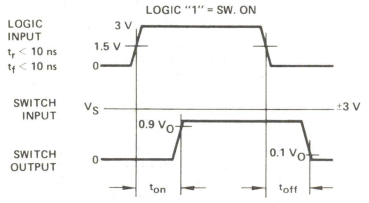
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

DG180 – DG185



DG186 – DG191





NOTE: LOGIC INPUT WAVEFORM IS INVERTED FOR SWITCHES THAT HAVE THE OPPOSITE LOGIC SENSE CONTROL

APPLICATION HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S Analog Voltage Range (V)
10 Ω	+15**	−15	+5	Gnd	2.0/0.8	−7.5 to +15
and	+10	−20	+5	Gnd	2.0/0.8	−12.5 to +10
30 Ω	+12	−12	+5	Gnd	2.0/0.8	−4.5 to +12
	+15**	−15	+5	Gnd	2.0/0.8	−10 to +15
75 Ω	+10	−20	+5	Gnd	2.0/0.8	−15 to +10
	+12	−12	+5	Gnd	2.0/0.8	−7 to +12

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Parameter Chart based on V+ = +15 V, V− = −15 V, V_L = 5 V, V_R = Gnd.

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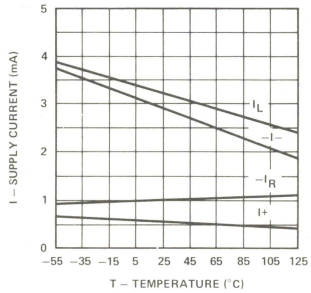
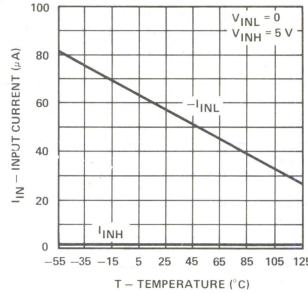
TYPICAL CHARACTERISTICS

Supply Current vs Temperature

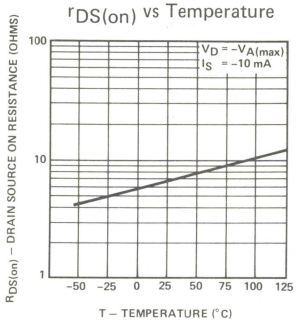


I_{IN} vs V_{IN} and Temperature

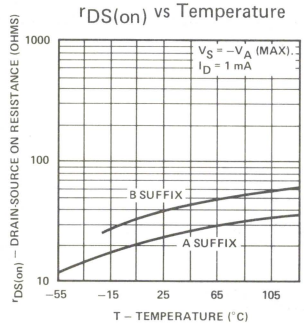


10 Ω	30 Ω	75 Ω
DG180	DG181	DG182
DG183	DG184	DG185
DG186	DG187	DG188
DG189	DG190	DG191

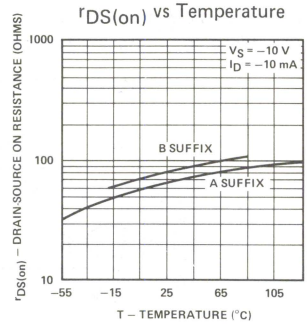
$r_{DS(on)}$ vs Temperature



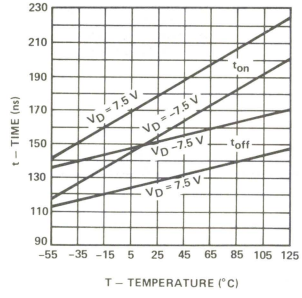
$r_{DS(on)}$ vs Temperature



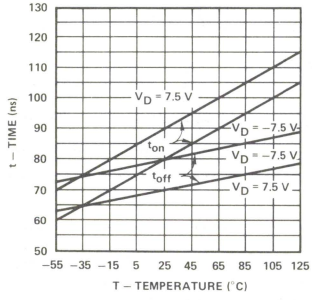
$r_{DS(on)}$ vs Temperature



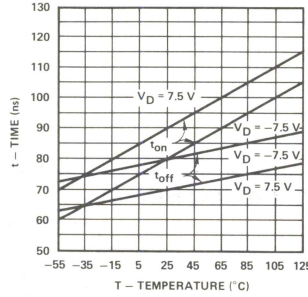
Switching Time vs V_D and Temperature



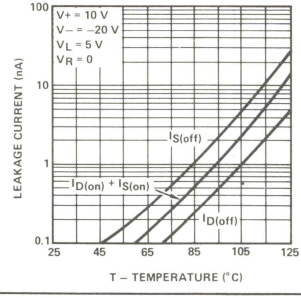
Switching Time vs V_D and Temperature



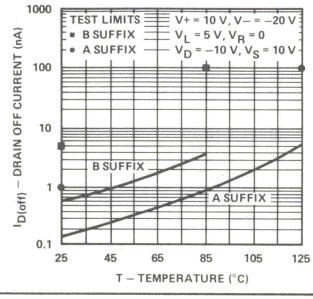
Switching Time vs V_D and Temperature



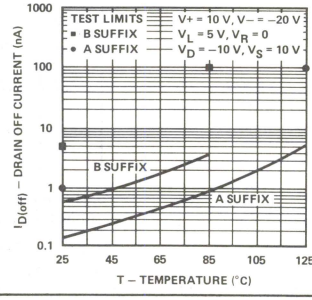
Leakage vs Temperature



$I_{D(off)}$ vs Temperature



$I_{D(off)}$ vs Temperature



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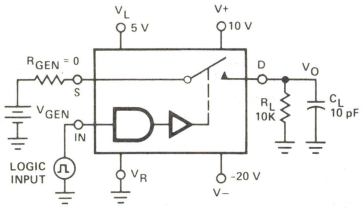
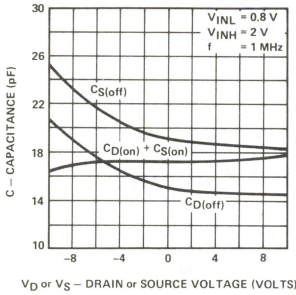
TYPICAL CHARACTERISTICS (Cont'd)

Typical delay, rise, fall, settling times, and switching transients in this circuit.

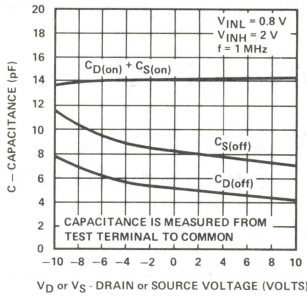


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall times.

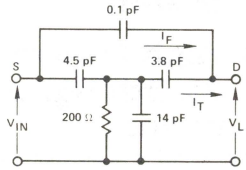
Capacitance vs V_D or V_S
10 Ω FET



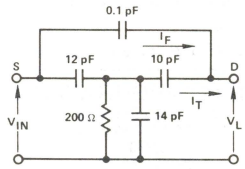
Capacitance vs V_D or V_S
30-75 Ω FET


V_{INL} = 0.8 V
V_{INH} = 2 V
f = 1 MHz
$C_{D(on)} + C_{S(on)}$
$C_{S(off)}$
$C_{D(off)}$
CAPACITANCE IS MEASURED FROM TEST TERMINAL TO COMMON
C – CAPACITANCE (pF)
V_D or V_S - DRAIN or SOURCE VOLTAGE (VOLTS)

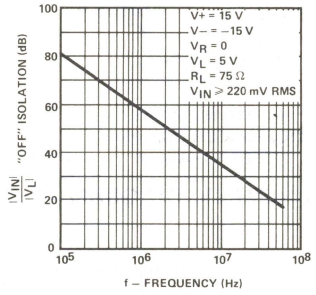
Equivalent "OFF" Circuit
30-75 Ω FET



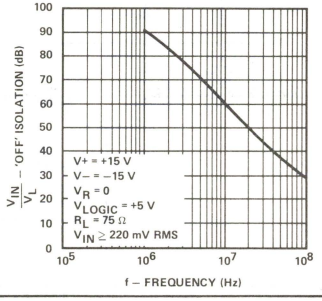
Equivalent "OFF" Circuit
10 Ω FET



"OFF" Isolation vs Frequency
10 Ω FET

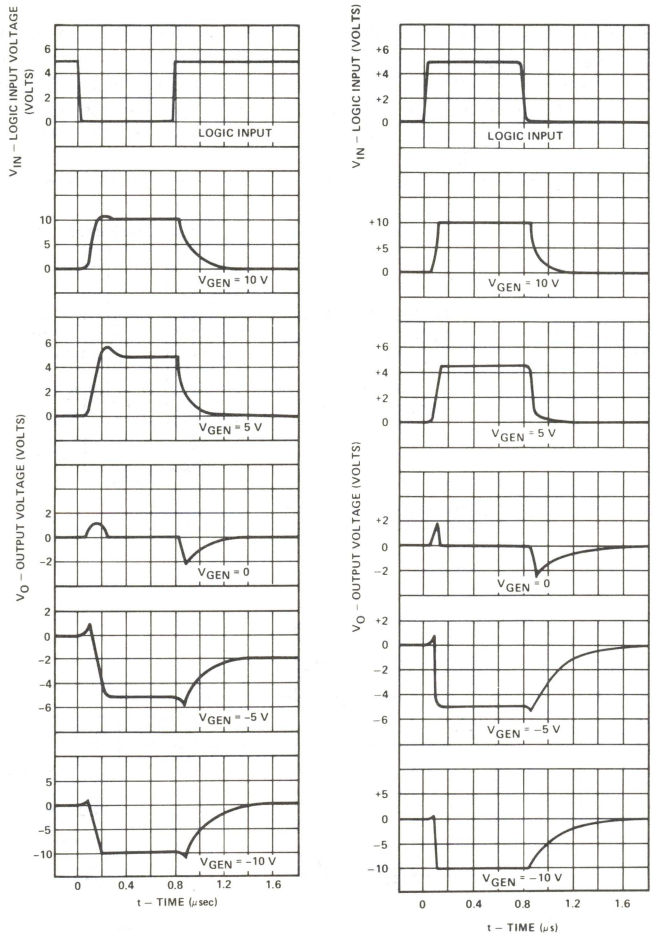


"OFF" Isolation vs Frequency
30-75 Ω FET



DG180, DG183, DG186
DG189

DG181, DG182, DG184,
DG185, DG187, DG188,
DG190, DG191


V_{IN} – LOGIC INPUT VOLTAGE (VOLTS)
LOGIC INPUT
V_{GEN} = 10 V
V_{GEN} = 5 V
V_{GEN} = 0
V_{GEN} = –5 V
V_{GEN} = –10 V
V_O – OUTPUT VOLTAGE (VOLTS)
t – TIME (μsec)
t – TIME (μs)

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Dual Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Low Transient Switching i.e. Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **TTL Compatible Switching Systems**
- **High Frequency Signal Switching, such as Video Signals**

BENEFITS

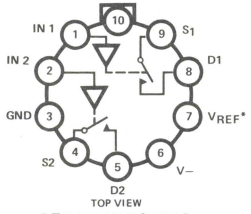
- **Environmentally Rugged**
  - Latch-proof CMOS
- **Easily Interfaced**
  - TTL, DTL and CMOS Direct Control Interface Over Military Temperature Range
- **Reduces External Component Requirements**
  - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
  - Break-Before-Make Switching
- **Eliminates Signal Error**
  - 10 pA Typical Leakage From Source or Drain
  - Low Charge Coupling

DESCRIPTION

The DG200 is a 2-channel, single-pole, single-throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make.

PIN CONFIGURATIONS

Metal Can Package
V+ (SUBSTRATE AND CASE)



TOP VIEW

ORDER NUMBERS:
DG200AA OR DG200BA
SEE PACKAGE 2

LOGIC	SWITCH
0	ON
1	OFF

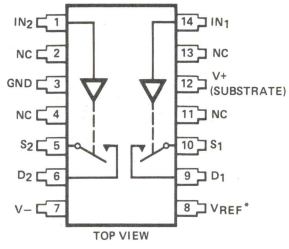
*Optional (Normally Left Open)

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ORDER NUMBERS:
DG200AP OR DG200BP
SEE PACKAGE 11

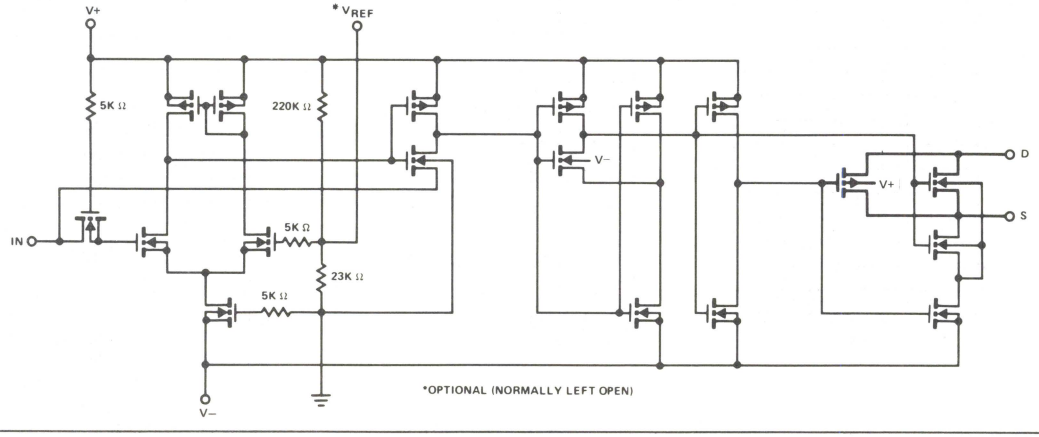
DG200CJ
SEE PACKAGE 7

Dual-In-Line Package



TOP VIEW

SCHEMATIC DIAGRAM (Typical Channel)



*OPTIONAL (NORMALLY LEFT OPEN)

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ABSOLUTE MAXIMUM RATINGS

V_{IN} and V_{REF} to Ground . . . . . −0.3 V, V+
V_S or V_D to V+ . . . . . 0, −32 V
V_S or V_D to V− . . . . . 0, 32 V
V+ to Ground . . . . . 16 V
V− to Ground . . . . . −16 V
Current, Any Terminal Except S or D . . . . 30 mA
Current, S or D . . . . . 20 mA
Current, S or D Pulsed
(1 msec, 10% Duty Cycle Max) . . . . . 100 mA
Operating Temp. (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
(C Suffix) . . . . . 0 to 70°C
Storage Temp. (A & B Suffix) . . . . −65 to 150°C
(C Suffix) . . . . . −65 to +125°C
Power Dissipation (Package)*
Metal Can** . . . . . 450 mW
14 Pin DIP*** . . . . . 825 mW
14 Pin Plastic DIP**** . . . . . 470 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C
***Derate 11 mW/°C above 75°C
****Derate 6.5 mW/°C above 25°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

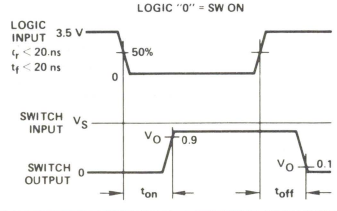
		CHARACTERISTIC		TYP† 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX −20/ 0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/ 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0, V_{REF} = Open***	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	45	70	70	100	80	80	100	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = −1 mA
3				45	70	70	100	80	80	100		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	+0.01		2	100		5	100	nA	V_S = 14 V, V_D = −14 V	V_{IN} = 2.4 V
5				−0.02		−2	−100		−5	−100		V_S = −14V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	+0.01		2	100		5	100		V_D = 14 V, V_S = −14 V	
7				−0.02		−2	−100		−5	−100		V_D = −14 V, V_S = 14 V	
8		$I_{D(on)}$*	Channel ON Leakage Current	+0.1		2	200		−5	200		V_D = V_S = 14 V	V_{IN} = 0.8 V
9				−0.1		−2	−200		−5	−200		V_D = V_S = −14 V	
10	INPUT	I_{INH}	Input Current Input Voltage High	0.0009		−1	−10		−1	−10	μA	V_{IN} = 2.4 V	
11				0.005		1	10		1	10		V_{IN} = 15 V	
12		$I_{IN(peak)}$	Peak Input Current Required for Transition	−150								See Curve I_{IN} vs V_{IN}	
13		I_{INL}	Input Current, Input Voltage Low	−.0015		−1	−10		−1	−10		V_{IN} = 0 V	
14	DYNAMIC	t_{on}	Turn-ON Time	440		1000			1000		ns	See Switching Time Test Circuit	
15		t_{off}	Turn-OFF Time	370		500			500				
16		$C_{S(off)}$	Source OFF Capacitance	9.0							pF	V_S = 0, V_{IN} = 5 V	
17		$C_{D(off)}$	Drain OFF Capacitance	9.0								V_D = 0, V_{IN} = 5 V	f = 140 kHz
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	25								V_D = V_S = 0, V_{IN} = 0	
19		OFF Isolation		72							dB	V_{IN} = 5 V, R_L = 1K Ω, C_L = 15 pF, V_S = 7 VRMS, f = 500 kHz	
20	SUP	I+	Positive Supply Current	+2.3		4			4		mA	Both Channels "ON," V_{IN} = 0	
21		I−	Negative Supply Current	−2.3		−4			−4				
22		I+ Standby	Positive Supply Current	+0.7		2			2			Both Channels "OFF," V_{IN} = 5 V	
23		I− Standby	Negative Supply Current	−0.6		−2			−2				

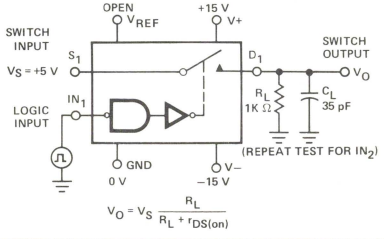
ICXE

NOTES:
†Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
*$I_{D(on)}$ is leakage from driver into "ON" switch.
**"OFF" isolation $\triangleq$ 20 log V_S/V_D. V_S = input to OFF switch, V_D = output
***Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift. For V+ = −V− = 10 V, 1.4 V may be applied to V_{REF} terminal. The V_{REF} terminal has $R_{IN} \cong$ 21K Ω. See Applications Section.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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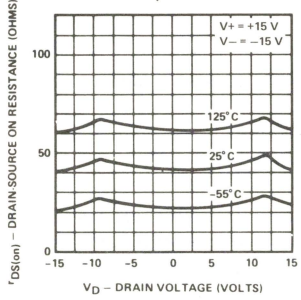
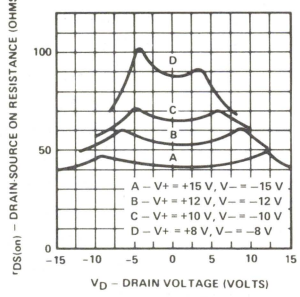
TYPICAL CHARACTERISTICS

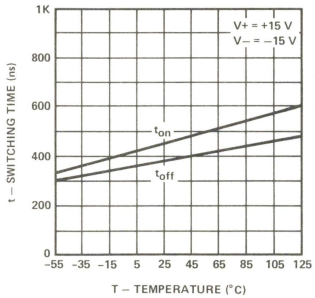
$r_{DS(on)}$ vs V_D and Temperature



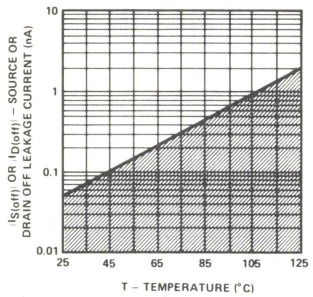
$r_{DS(on)}$ vs V_D and Power Supply Voltage


D
C
B
A
A – V+ = +15 V, V− = −15 V
B – V+ = +12 V, V− = −12 V
C – V+ = +10 V, V− = −10 V
D – V+ = +8 V, V− = −8 V
100
50
0
−15 −10 −5 0 5 10 15
rDS(on) – DRAIN-SOURCE ON RESISTANCE (OHMS)
VD – DRAIN VOLTAGE (VOLTS)

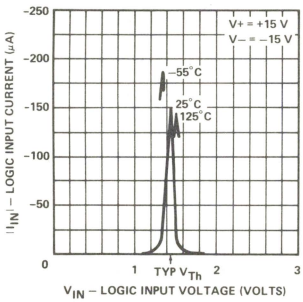
Switching Time vs Temperature



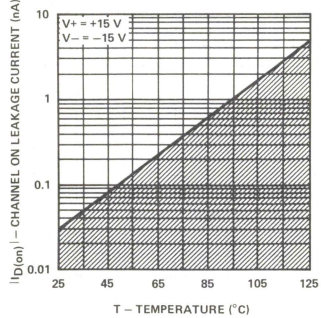
$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*



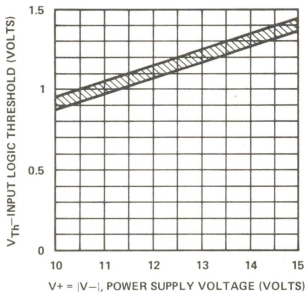
I_{IN} vs V_{IN}



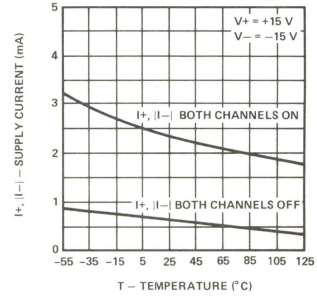
$I_{D(on)}$ vs Temperature*



V_{Th} (Input Logic Threshold) vs Power Supply Voltage

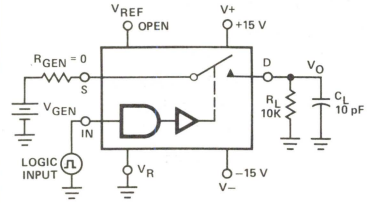


Supply Current vs Temperature

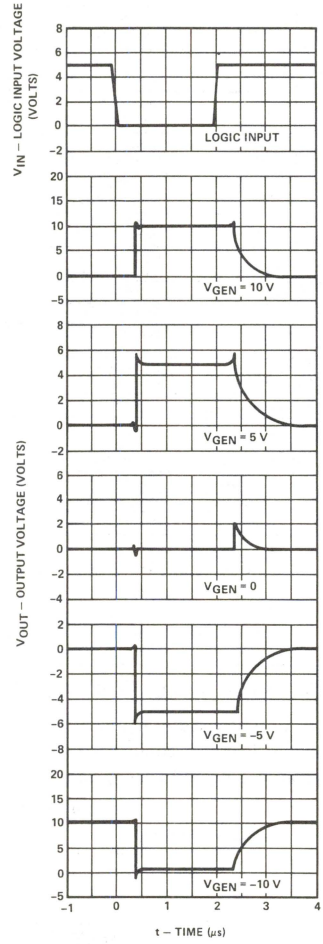


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.


VIN – LOGIC INPUT VOLTAGE (VOLTS)
LOGIC INPUT
VGEN = 10 V
VGEN = 5 V
VGEN = 0
VGEN = −5 V
VGEN = −10 V
VOUT – OUTPUT VOLTAGE (VOLTS)
−1 0 1 2 3 4
t – TIME (μs)

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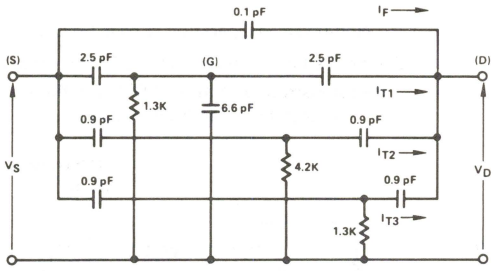
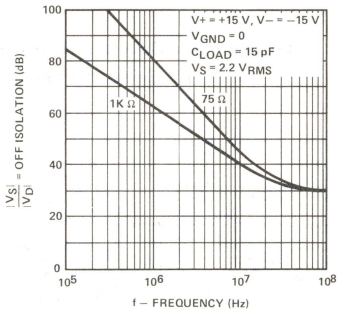
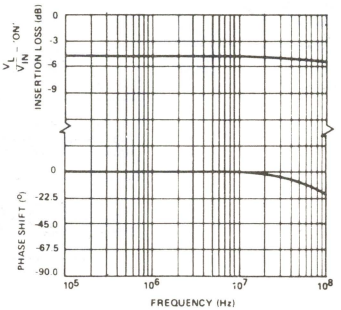
TYPICAL CHARACTERISTICS (Cont'd)

"OFF" Isolation Equivalent Circuit and Data







APPLICATIONS

Application Hints*

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	–15	Open	2.4/0.8	–15 to +15
+12	–12	Open or 1.4 V	2.4/0.8	–12 to +12
+10	–10	1.4 V	2.4/0.8	–10 to +10
+8***	–8	1.4 V	2.4/0.8	–8 to +8

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V– = –15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended.

Logic Inputs

Logic input circuitry protects the input MOS gate from static transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection, it should be limited to less than 4.7 KΩ to insure switching with worst case current spikes.

The Function of V_{REF}

V_{REF} is an internal connection which allows the user to establish the logic threshold voltage at which the switch changes state. The actual threshold voltage is equal to the voltage on the V_{REF} pin. V_{REF} is internally connected for a 1.4 V threshold at V+ = +15 V. For other thresholds and/or supply voltages, one may connect V_{REF} to a voltage source or resistive divider whose output voltage is equal to the desired threshold. The internal impedance of V_{REF} is 21 KΩ ±30%.

Additionally, to adjust V_{REF}, a single pullup resistor can be used from the V_{REF} pin to a positive supply voltage to shunt the upper internal divider resistor. The equation below shows the calculation of the shunt resistor for the desired logic threshold voltage – this calculation is based on nominal internal resistor values, which are ±30% in absolute magnitude. The adjusted trip point voltage (V_{REF}) should be limited to an upper level of 5 V to avoid input logic switching transition hysteresis.

$$R_{SHUNT} = \frac{R1 \times R2\left(\frac{V^+}{V_{tr}} - 1\right)}{\left[R1 - R2\left(\frac{V^+}{V_{tr}} - 1\right)\right]}$$

Calculation of R_{SHUNT}

Where $R1 \simeq 220$ KΩ: nominal values,
$R2 \simeq 23$ KΩ ±30% run to run

Example: for V+ = 15 V, V_{TRIP} = 5 V, using nominal R1, R2 calc R_{SHUNT} = 58 KΩ.

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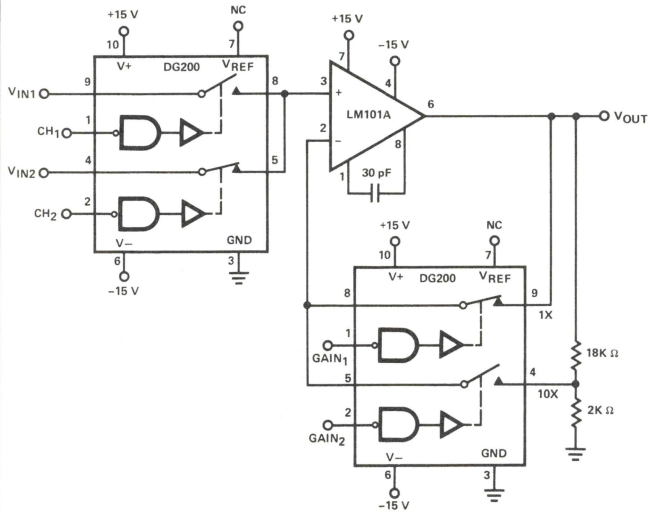
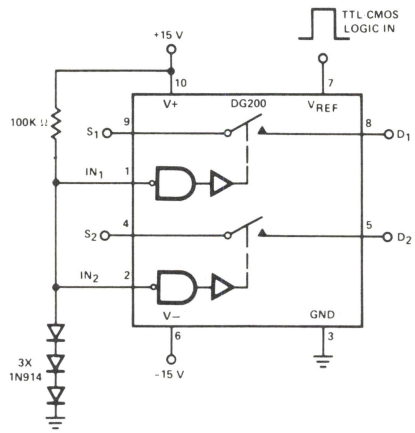
APPLICATIONS (Cont'd)

Programmable Gain Non-Inverting Amplifier with Selectable Inputs



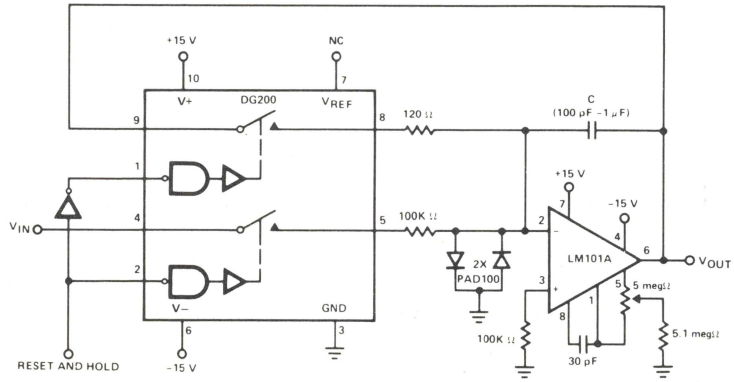
Non-Inverted Operation (Logic 1 = ON)

Can be used with a second DG200 connected in the standard way to make a DPDT without the need for an additional inverter.



NOTE: Both channels switch simultaneously

Integrator Reset



$$V_O = \frac{10}{C}\int_{t_1}^{t_2} V_{IN}\,dt \qquad (C \text{ in } \mu F)$$

NOTE: Pin connections shown for metal can package

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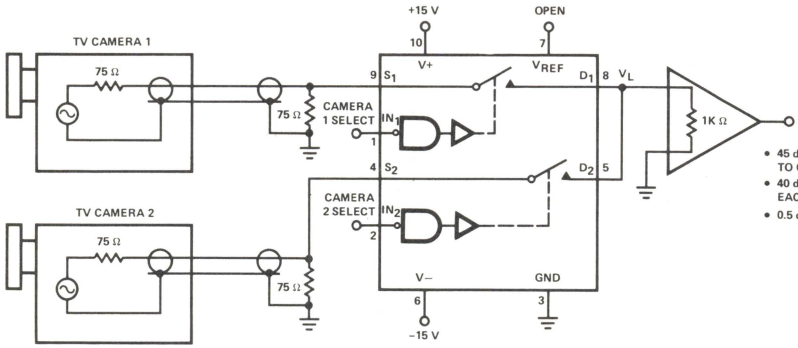
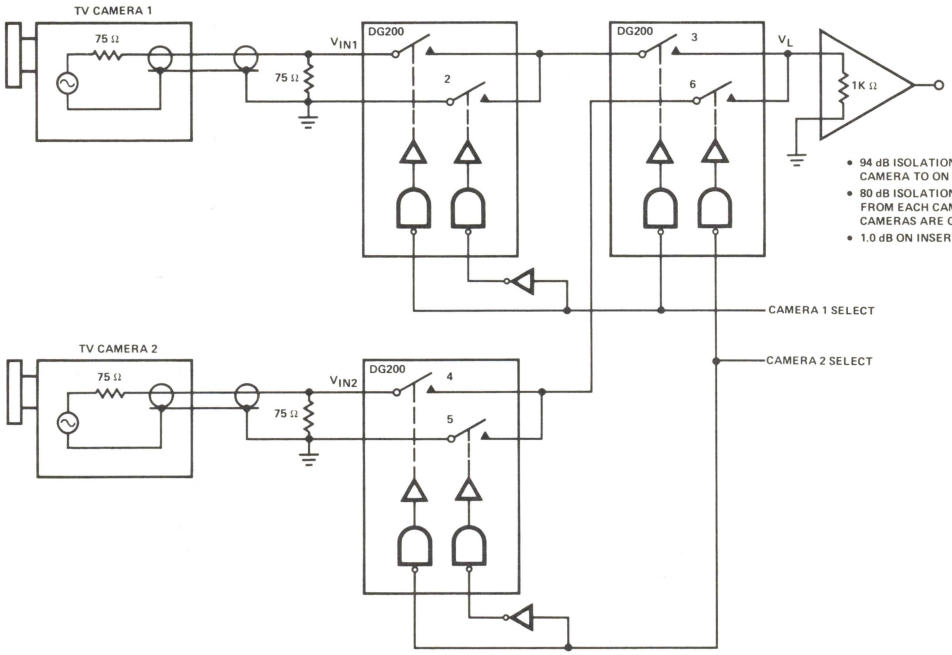
APPLICATIONS (Cont'd)

VIDEO SWITCH
(f = DC to 10 MHz)



- 45 dB ISOLATION Δ T 10 MHz OFF CAMERA TO ON CAMERA
- 40 dB ISOLATION AT 10 MHz, LOAD FROM EACH CAMERA WHEN BOTH ARE OFF
- 0.5 dB ON INSERTION LOSS

VIDEO SWITCH WITH VERY HIGH OFF ISOLATION
(f = DC to 10 MHz)



- 94 dB ISOLATION AT 10 MHz OFF CAMERA TO ON CAMERA
- 80 dB ISOLATION AT 10 MHz LOAD FROM EACH CAMERA WHEN BOTH CAMERAS ARE OFF
- 1.0 dB ON INSERTION LOSS

NOTE: Pin connections shown are for metal can package

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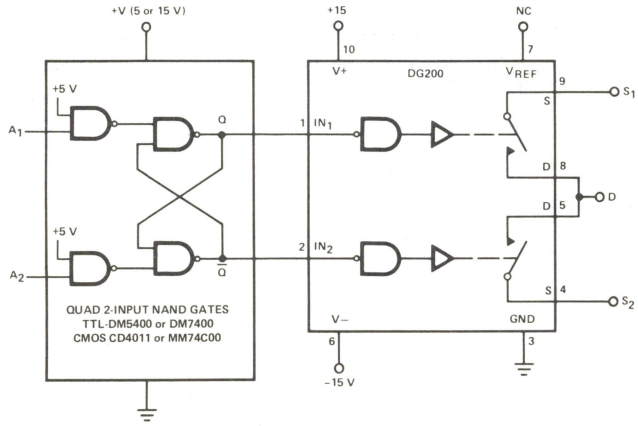
APPLICATIONS (Cont'd)

A Latching SPDT

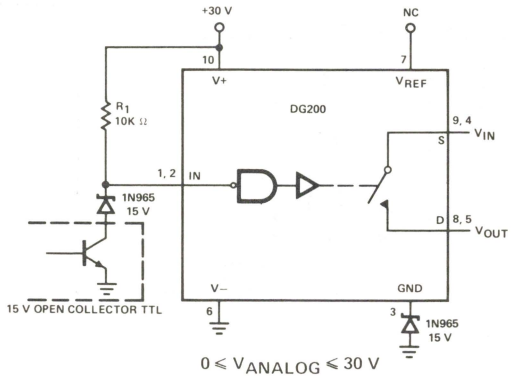
The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_1 turns S_2 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.



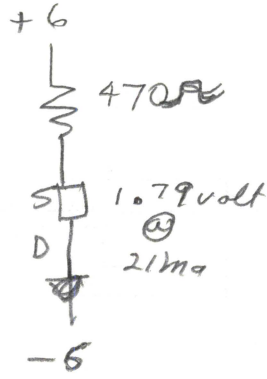
TRUTH TABLE

COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_2	S_1
0	0 (normal)	same	same
0	1	ON	OFF
1	0	OFF	ON
1	1	INDETERMINATE	

Operation From a Unipolar Supply



$0 \leqslant V_{ANALOG} \leqslant 30$ V



NOTE: Pin connections shown for metal can package

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Quad Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Low Transient Switching i.e. Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **High Frequency Signal Switching**
- **TTL Compatible Systems**

BENEFITS

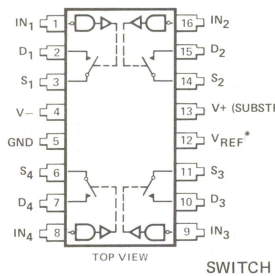
- **Environmentally Rugged**
  - Latch-proof CMOS
- **Reduced Switching Error**
  - Low Charge Coupling
- **Easily Interfaced**
  - TTL, DTL and CMOS Direct Control Interface Over Military Temperature Range
- **Reduces External Component Requirements**
  - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
  - Break-Before-Make Switching
- **Eliminates Signal Error**
  - 10 pA Typical Leakage From Source or Drain

DESCRIPTION

The DG201 is a 4-channel single pole signal throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make.

PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DG201AP OR DG201BP
SEE PACKAGE 12

DG201CJ
SEE PACKAGE 8

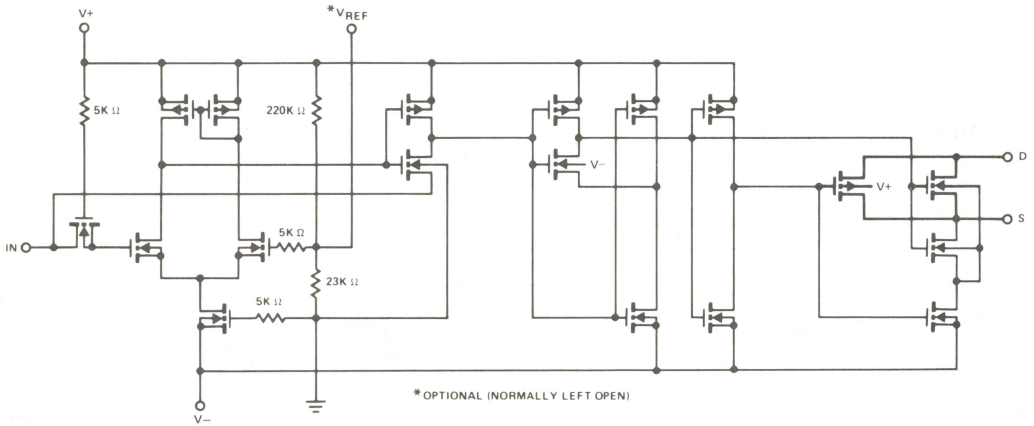
LOGIC	SWITCH
0	ON
1	OFF

20ma

*Optional (Normally Left Open)

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

SCHEMATIC DIAGRAM (Typical Channel)



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ABSOLUTE MAXIMUM RATINGS

V_{IN} and V_{REF} to Ground . . . . . −0.3 V, V+
V_S or V_D to V+ . . . . . 0, −32 V
V_S or V_D to V− . . . . . 0, 32 V
V+ to Ground . . . . . 16 V
V− to Ground . . . . . −16 V
Current, Any Terminal Except S or D . . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(pulsed at 1 msec, 10% duty cycle max) . . 70 mA
Storage Temperature (A & B Suffix) . . −65 to 150°C
(C Suffix) . . . . −65 to 125°C
Operating Temperature (A Suffix) . . . −55 to 125°C
(B Suffix) . . . −20 to 85°C
(C Suffix) . . . 0 to 70°C
Power Dissipation (Package)*
16 Pin DIP** . . . . . 900 mW
16 Pin Plastic DIP*** . . . . . 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		TYP† 25°C	MAX LIMITS A SUFFIX −55°C	MAX LIMITS A SUFFIX 25°C	MAX LIMITS A SUFFIX 125°C	MAX LIMITS B/C SUFFIX −20°C/0°C	MAX LIMITS B/C SUFFIX 25°C	MAX LIMITS B/C SUFFIX 85°C/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0, V_{REF} = Open***	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	115	175	175	250	200	200	250	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = −1 mA
3				75	175	175	250	200	200	250		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	0.01		1	100		5	100	nA	V_S = 14 V, V_D = −14V	V_{IN} = 2.4 V
5				−0.02		−1	−100		−5	−100		V_S = −14V, V_D = 14V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.01		1	100		5	100		V_D = 14V, V_S = −14V	
7				−0.02		−1	−100		−5	−100		V_D = −14V, V_S = 14V	
8		$I_{D(on)}$*	Drain ON Leakage Current	0.1		1	200		5	200		V_D = V_S = 14V	V_{IN} = 0.8 V
9				−0.15		−1	−200		−5	−200		V_D = V_S = −14V	
10	INPUT	I_{INH}	Input Current, Input Voltage High	−.0004		−1	−10		−1	−10	μA	V_{IN} = 2.4 V	
11				.003		1	10		1	10		V_{IN} = 15 V	
12		$I_{IN(peak)}$	Peak Input Current Required for Transition	−120								See Curve I_{IN} vs V_{IN}	
13		I_{INL}	Input Current, Input Voltage Low	−.0004		−1	−10		−1	−10		V_{IN} = 0	
14		t_{on}	Turn-ON Time	580		1000					ns	See Switching Time Test Circuit	
15		t_{off}	Turn-OFF Time	370		500							
16	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	7							pF	V_S = 0, V_{IN} = 5 V	f = 140 KHz
17		$C_{D(off)}$	Drain OFF Capacitance	7								V_D = 0, V_{IN} = 5 V	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	20								V_D = V_S = 0, V_{IN} = 0	
19		Off Isolation**		54							dB	V_{IN} = 5 V, R_L = 1K Ω, C_L = 20 pF, V_S = 7 VRMS, f = 500 kHz	
20	SUPPLY	I+	Positive Supply Current	2.1		4.0			4.0		mA	One Channel "ON," V_{IN} = 0	
21		I−	Negative Supply Current	−2.1		−4.0			−4.0				
22		I+ Standby	Positive Supply Current	1.4		3.0			3.0			All Channels "OFF," V_{IN} = 5 V	
23		I− Standby	Negative Supply Current	−1.4		−3.0			−3.0				

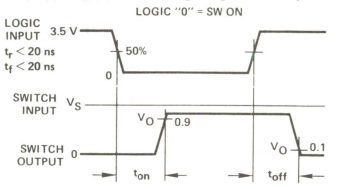
†Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing. ICXF

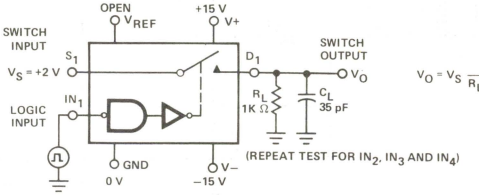
*$I_{D(on)}$ is leakage from driver into "ON" switch. **"OFF" Isolation = $20 \log \frac{|V_S|}{|V_D|}$

***Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift. For V+ = |V−| = 10 V, +1.4 V may be applied to the V_{REF} terminal. The V_{REF} terminal has $R_{IN} \cong$ 21K Ω. See the Applications Section.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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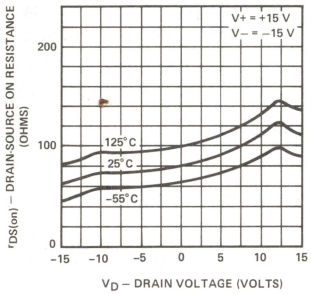
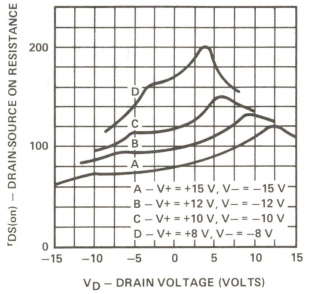
TYPICAL CHARACTERISTICS

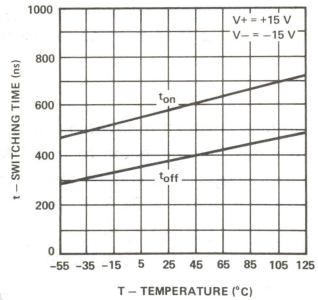
$r_{DS(on)}$ vs V_D and Temperature



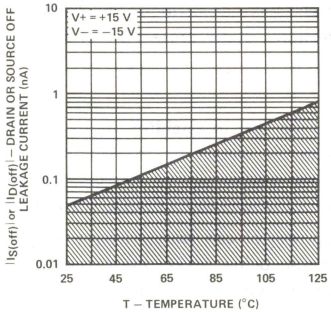
$r_{DS(on)}$ vs V_D and Power Supply Voltage


D
C
B
A
A – V+ = +15 V, V– = –15 V
B – V+ = +12 V, V– = –12 V
C – V+ = +10 V, V– = –10 V
D – V+ = +8 V, V– = –8 V
200
100
0
–15 –10 –5 0 5 10 15
rDS(on) – DRAIN-SOURCE ON RESISTANCE
VD – DRAIN VOLTAGE (VOLTS)

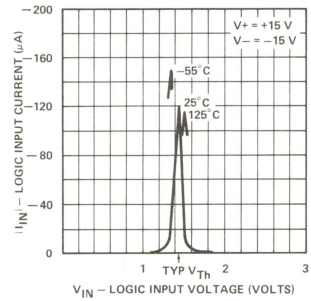
Switching Time vs Temperature



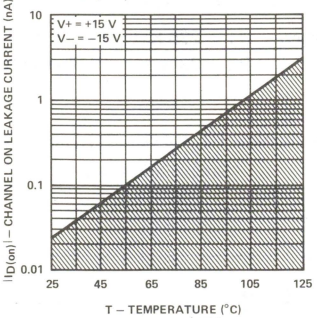
$I_{D(off)}$ or $I_{S(off)}$ vs Temperature*



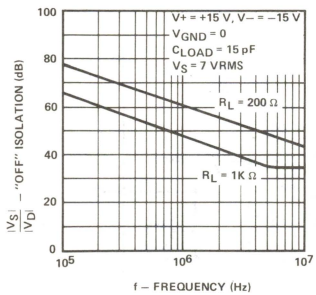
I_{IN} vs V_{IN}



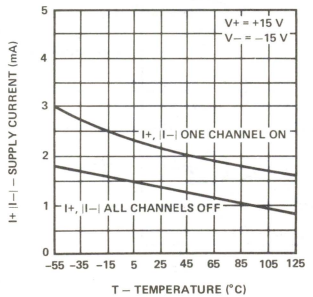
$I_{D(on)}$ vs Temperature*



OFF Isolation vs Frequency

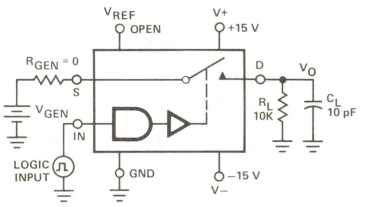


Supply Current vs Temperature

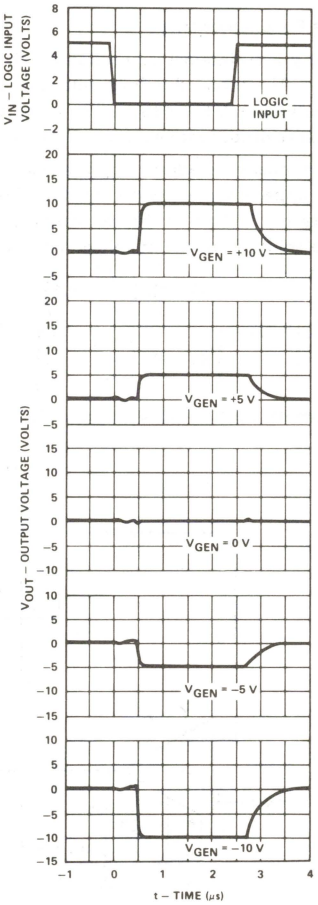


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater t_{on} spikes.


VIN – LOGIC INPUT VOLTAGE (VOLTS)
LOGIC INPUT
VGEN = +10 V
VGEN = +5 V
VGEN = 0 V
VGEN = –5 V
VGEN = –10 V
VOUT – OUTPUT VOLTAGE (VOLTS)
–1 0 1 2 3 4
t – TIME (μs)

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APPLICATIONS

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V− = −15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended.

Application Hints*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	−15	Open	2.4/0.8	−15 to +15
+12	−12	Open or 1.4 V	2.4/0.8	−12 to +12
+10	−10	1.4 V	2.4/0.8	−10 to +10
+8***	−8	1.4 V	2.4/0.8	−8 to +8

Logic Inputs

Logic input circuitry protects the input MOS gate from static transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection, it should be limited to less than 5.6 KΩ to insure switching with worst case current spikes.

The Function of V_{REF}

V_{REF} is an internal connection which allows the user to establish the logic threshold voltage at which the switch changes state. The actual threshold voltage is equal to the voltage on the V_{REF} pin. V_{REF} is internally connected for a 1.4 V threshold at V+ = +15 V. For other thresholds and/or supply voltages, one may connect V_{REF} to a voltage source or resistive divider whose output voltage is equal to the desired threshold. The internal impedance of V_{REF} is 21 KΩ ±30%.

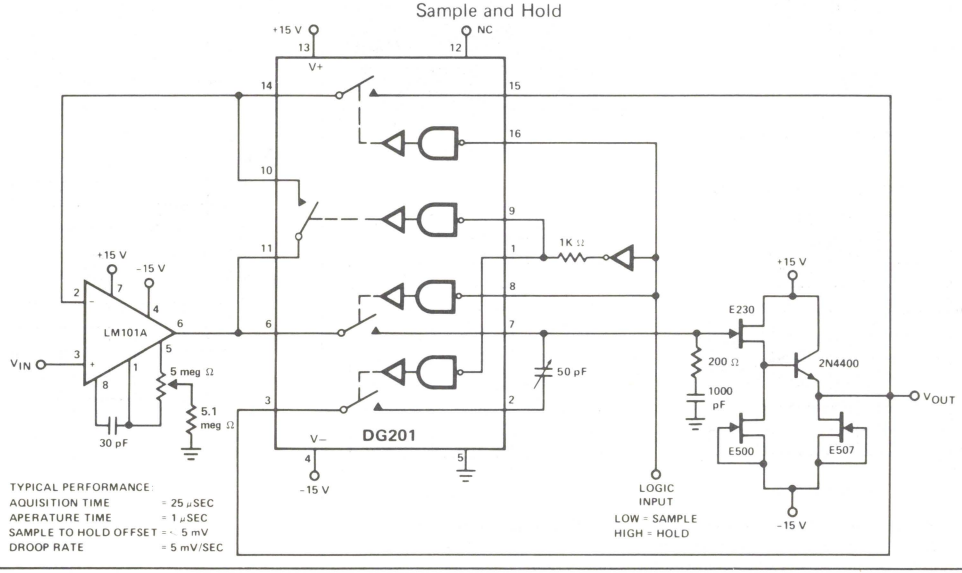
Additionally, to adjust V_{REF}, a single pullup resistor can be used from the V_{REF} pin to a positive supply voltage to shunt the upper internal divider resistor. The equation below shows the calculation of the shunt resistor for the desired logic threshold voltage — this calculation is based on nominal internal resistor values, which are ±30% in absolute magnitude. The adjusted trip point voltage (V_{REF}) should be limited to an upper level of 5 V to avoid input logic switching transition hysteresis.

$$R_{SHUNT} = \frac{R1 \times R2\left(\frac{V^+}{V_{tr}} - 1\right)}{\left[R1 - R2\left(\frac{V^+}{V_{tr}} - 1\right)\right]}$$

Calculation of R_{SHUNT}

Where $R1 \simeq 220$ KΩ nominal values,
$R2 \simeq 23$ KΩ ±30% run to run

Example: for V+ = 15 V, V_{TRIP} = 5 V, using nominal R1, R2 calc R_{SHUNT} = 58 KΩ.



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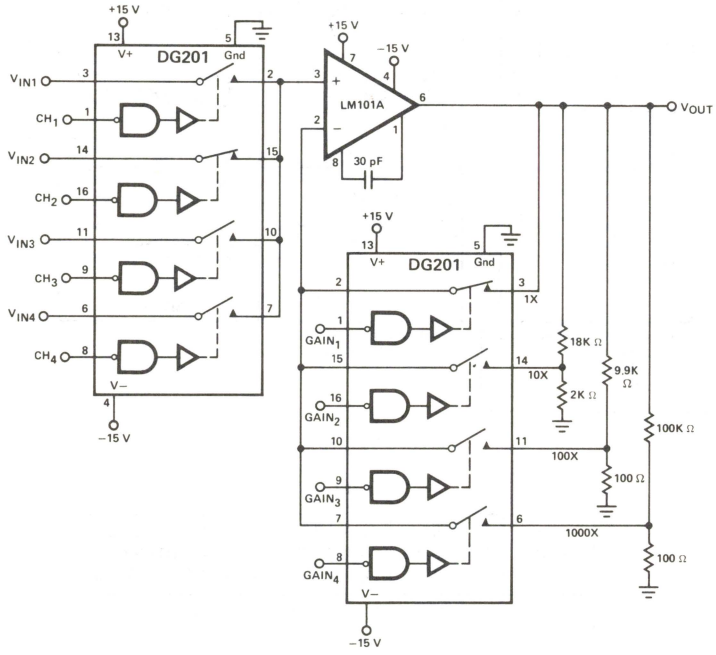
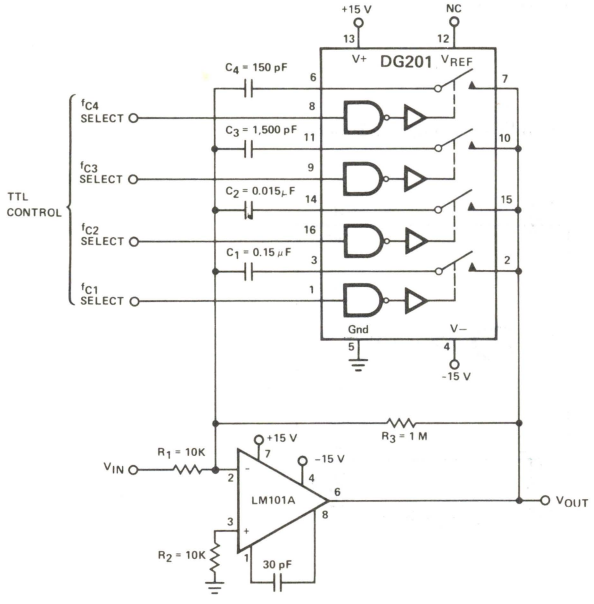
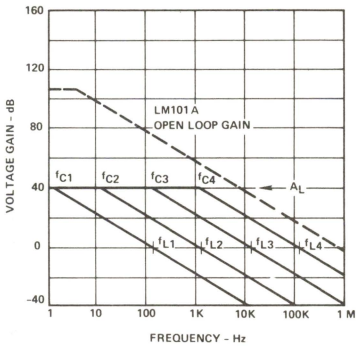
APPLICATIONS (Continued)

Programmable Gain Non-Inverting Amplifier
with Selectable Inputs



Active Low Pass Filter with Digitally
Selected Break Frequency





A_L (VOLTAGE GAIN BELOW BREAK FREQUENCY)
$= \frac{R_3}{R_1} = 100$ (40 dB)

f_c (BREAK FREQUENCY) $= \frac{1}{2\pi R_3 C_X}$

f_L (UNITY GAIN FREQUENCY) $= \frac{1}{2\pi R_1 C_X}$

MAX ATTENUATION $= \frac{r_{DS(on)}}{10K} \approx -40$ dB

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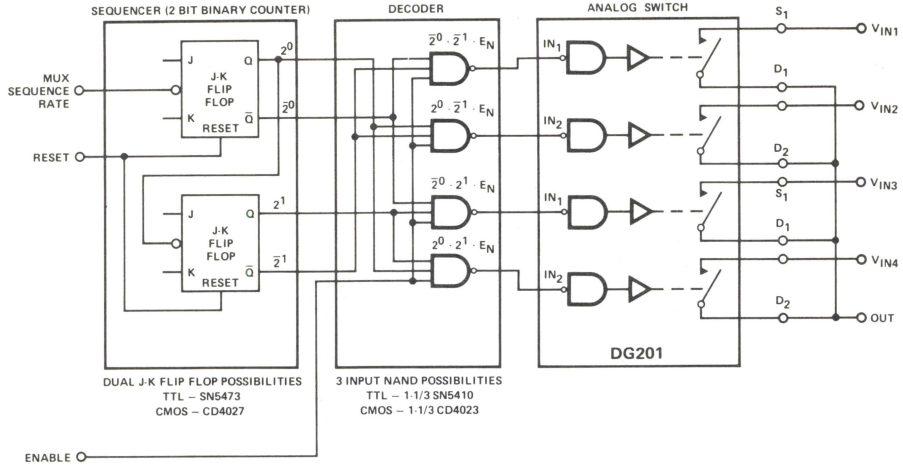
APPLICATIONS (Continued)

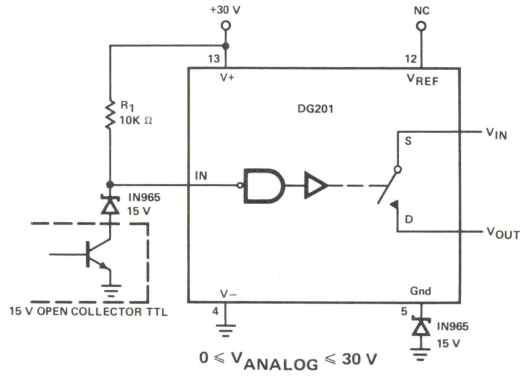
4-Channel Sequencing MUX



Truth Table

ENABLE	MUX SEQUENCE RATE	SEQUENCER OUTPUT 2^0	SEQUENCER OUTPUT 2^1	SWITCH STATES (– DENOTES OFF) SW1	SW2	SW3	SW4
0	0	0	0	–	–	–	–
1	0	0	0	ON	–	–	–
1	1 pulse	1	0	–	ON	–	–
1	2 pulses	0	1	–	–	ON	–
1	3 pulses	1	1	–	–	–	ON
1	4 pulses	0	0	ON	–	–	–

Operation From a Unipolar Supply



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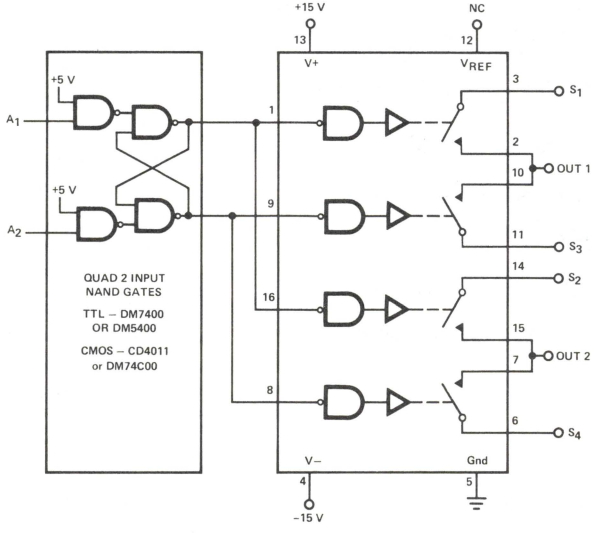
APPLICATIONS (Continued)

A Latching DPDT

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.



Truth Table

Command		State of Switches After Command	
A_2	A_1	S_3 & S_4	S_1 & S_2
0	0	same	same
0	1	on	off
1	0	off	on
1	1	INDETERMINATE	

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Quad Monolithic SPST CMOS Analog Switch

Siliconix

ADVANCE INFORMATION

designed for . . .

- **Low Transient Switching i.e., Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **High Frequency Signal Switching e.g., Computer Peripheral Equipment**
- **TTL Compatible Systems Including Microprocessor Systems**

BENEFITS

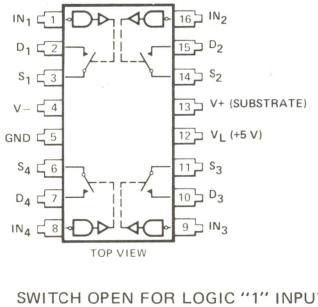
- **Environmentally Rugged**
  - Latchproof
  - Operation up to 40 V
- **Reduced Switching Error**
  - Low Charge Coupling
- **Easily Interfaced**
  - TTL, DTL and CMOS Direct Control Interface Over Military Temperature Range
- **Reduces External Component Requirements**
  - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
  - Break-Before-Make Switching
- **Eliminates Signal Error**
  - 0.01 nA Typical Leakage From Source Or Drain
- **Pin for Pin Compatible with Intersil IH5052**
- **Low Cost**

DESCRIPTION

The DG211 is a 4-channel single pole single throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

LOGIC	SWITCH
0	ON
1	OFF

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

TENTATIVE DATA SHEET

This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.

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Siliconix

ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground . . . . . V−, V+
V_S or V_D to V+ . . . . . 0, −40 V
V_S or V_D to V− . . . . . 0, 40 V
V+ to Ground . . . . . 20 V
V− to Ground . . . . . −20 V
Current, Any Terminal Except S or D . . . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(pulsed at 1 msec, 10% duty cycle max) . . . . . 70 mA
Storage Temperature (A & B Suffix) . . . . . −65 to 150°C
(C Suffix) . . . . . −65 to 125°C
Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
(C Suffix) . . . . . 0 to 70°C
Power Dissipation (Package)*
16 Pin DIP** . . . . . 900 mW
16 Pin Plastic DIP*** . . . . . 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		PROPOSED MAX LIMITS C SUFFIX		UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0, V_L = 5 V	
				TYP[1] 25°C	25°C			
1	SWITCH	V_{ANALOG}	Min. Analog Signal Handling Capability	±15	±15	V	I_S = 10 mA When ON	
2		$r_{DS(on)}$	Drain Source ON Resistance	125	175	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = −1 mA
3				115	175		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	0.01	1	nA	V_S = 14 V, V_D = −14 V	V_{IN} = 2.4 V
5				−0.02	−1		V_S = −14 V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.01	1		V_D = 14 V, V_S = −14 V	
7				−0.02	−1		V_D = −14 V, V_S = 14 V	
8		$I_{D(on)}$[2]	Drain ON Leakage Current	0.1	1		V_D = V_S = 14 V	V_{IN} = 0.8 V
9				−0.15	−1		V_D = V_S = −14 V	
10	INPUT	I_{INH}	Input Current, Input Voltage High	−0.0004	−1	µA	V_{IN} = 2.4 V	
11				0.003	1		V_{IN} = 15 V	
12		I_{INL}	Input Current, Input Voltage Low	−0.0004	−1		V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn-ON Time	420	500	ns	V_S = 2 V, R_L = 1K Ω, C_L = 35 pF	See Switching Time Test Circuit
14		t_{off1}	Turn-OFF Time	360	400			
15		t_{off2}	Turn-OFF Time	390				
16		$C_{S(off)}$	Source OFF Capacitance	7		pF	V_S = 0, V_{IN} = 5 V	f = 1 MHz
17		$C_{D(off)}$	Drain OFF Capacitance	7			V_D = 0, V_{IN} = 5 V	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	20			V_D = V_S = 0, V_{IN} = 0	
19		OFF Isolation[3]		50		dB	V_{IN} = 5 V, R_L = 1K Ω, C_L = 15 pF, V_S = 2 VRMS, f = 1 MHz	
20		Interchannel Crosstalk Isolation		50		dB		
21	SUP	I+	Positive Supply Current	0.25	0.4	mA	V_{IN} = 0 or 2.4 V	
22		I−	Negative Supply Current	0.22	0.4			
23		I_L	Logic Supply Current	0.5	1.2			

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into ON switch.
3. OFF Isolation = $20 \log \frac{|V_S|}{|V_D|}$, V_S = input to OFF switch, V_D = output.

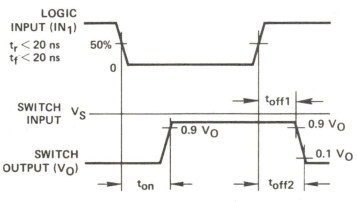
TENTATIVE DATA SHEET

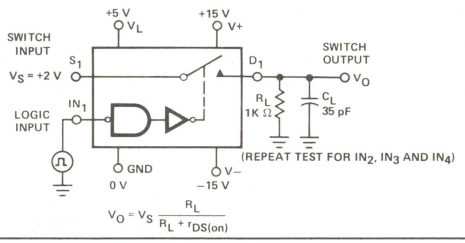
ICMC-A

This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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Low-Charge Coupling JFET Analog Switches *designed for...*

Siliconix

- **Low Error Sample and Hold Circuits**
- **100 MHz Signal Switching with High OFF Isolation**
- **Presettable Integrators with Minimum Offset Error**
- **Low Distortion Click Free Audio Switching**

BENEFITS

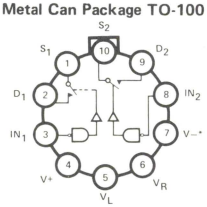
- **Minimum Signal Errors**
  - Low Charge Feedthrough 7 Picocoulombs Typical
  - Low "r_{on} x $I_{D(OFF)}$ Error Factor
  - Low Leakage Less Than 10 Picoamps Typical
  - Low Distortion — Constant ON Resistance
- **Easily Interfaced**
  - TTL and CMOS Logic Compatibility Over Full Temperature Range
- **Compact Circuit Layouts**
  - Several Form Factors Available in Single Packages (eg. 2XSPST, SPDT, 2XSPDT, 2XDPST)

DESCRIPTION

The DG281 series incorporates N-channel junction-type field-effect transistors (JFETs) designed to function as electronic switches. Level-shifting drivers enable TTL or CMOS outputs to control the ON-OFF state of each switch. The driver is designed to provide break-before-make action when switching from one channel to another. The low switch capacitance results in a minimal amount of charge-feedthrough into the analog signal path. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block voltages up to 22.5 V peak-to-peak.

PIN CONFIGURATIONS (Top View)

Metal Can Package TO-100

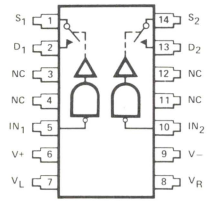


DUAL SPST

LOGIC	SW 1 & 2
0	ON
1	OFF

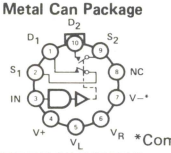
ORDER NUMBERS:
DG281AA OR DG281BA
SEE PACKAGE 2

Dual-In-Line Package TO-116



ORDER NUMBERS:
DG281AP OR DG281BP
SEE PACKAGE 11

Metal Can Package



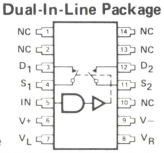
SPDT

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*Common to Substrate and Case

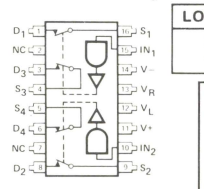
ORDER NUMBERS:
DG287AA OR DG287BA
SEE PACKAGE 2

Dual-In-Line Package



ORDER NUMBERS:
DG287AP OR DG287BP
SEE PACKAGE 11

Dual-In-Line Package



ORDER NUMBERS:
DG284AP OR DG284BP
SEE PACKAGE 12

DUAL DPST

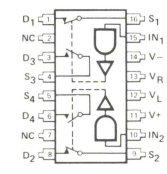
LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

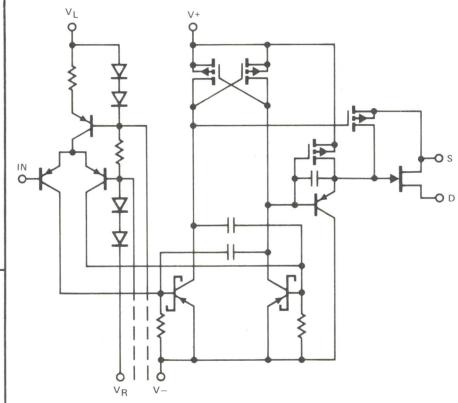
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Dual-In-Line Package



ORDER NUMBERS:
DG290AP OR DG290BP
SEE PACKAGE 12

SCHEMATIC DIAGRAM (Typical Channel)



APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S Analog Voltage Range (V)
+15**	-15	+5	Gnd	2.0/0.8	-7.5 to +15
+10	-20	+5	Gnd	2.0/0.8	-12.5 to +10
+12	-12	+5	Gnd	2.0/0.8	-4.5 to +12

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Parameter Chart based on V+ = +15 V, V− = −15 V, V_L = 5 V, V_R = Gnd.

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ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	33 V
V_D to V−	33 V
V_D to V_S	±22 V
V_L to V−	36 V
V_L to V_{IN}	8 V
V_L to V_R	8 V
V_{IN} to V_R	8 V
V_R to V−	27 V
V_R to V_{IN}	8 V
Current (Any Terminal)	20 mA
Storage Temperature	−65 to +150°C
Operating Temperature (A Suffix)	−55 to +125°C
(B Suffix)	−20 to +85°C

Power Dissipation*

Metal Can**	450 mW
14 Pin DIP***	825 mW
16 Pin DIP****	900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.
****Derate 12 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS DG281A, DG284A DG287A, DG290A −55°C	25°C	125°C	MAX LIMITS DG281B, DG284B DG287B, DG290B −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, V_L = 5 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance		300	500		300	500	Ω	V_D = −7.5 V	I_S = −1 mA††
2	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		0.5	100		2	100	nA	V_S = 7.5 V, V_D = −7.5 V	††
3	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current		0.2	100		1	100	nA	V_D = 7.5 V, V_S = −7.5 V	††
4	SWITCH	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		−2	−200		−10	−200	nA	V_D = V_S = −7.5 V	††
5	IN	I_{INL}	Input Current, Input Voltage Low	−250	−250	−250	−250	−250	−250	µA	V_{IN} = 0	
6	IN	I_{INH}	Input Current, Input Voltage High		10	20		10	20	µA	V_{IN} = 5 V	
7	DYNAMIC	t_{on}	Turn-ON Time		150			180		ns	See Switching Time Test Circuit	
8	DYNAMIC	t_{off}	Turn-OFF Time		130			150		ns	See Switching Time Test Circuit	
9	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	6 Typical*						pF	V_S = −5 V, I_D = 0	f = 1 MHz
10	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	2 Typical*						pF	V_D = −5 V, I_S = 0	f = 1 MHz
11	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	14-17 Typical*						pF	V_D = V_S = 0	f = 1 MHz
12	DYNAMIC	ΔQ	Charge-Feedthrough	11 Typical*						pC	V_S = 7.5 V	See Charge-Feedthrough Test Circuit
13	DYNAMIC	ΔQ	Charge-Feedthrough	4 Typical						pC	V_S = −7.5 V	See Charge-Feedthrough Test Circuit

POWER SUPPLY CURRENTS

		CHARACTERISTIC 25°C MAX LIMITS		DG281	DG284	DG287	DG290	UNIT	TEST CONDITIONS
14	SUPPLY	I_+	Positive Supply Current	1.5	3	0.8	0.8	mA	V_{IN} = 0†
15	SUPPLY	I_-	Negative Supply Current	−5	−5.5	−3	−3	mA	V_{IN} = 0†
16	SUPPLY	I_L	Logic Supply Current	4.5	4.5	3.2	3.2	mA	V_{IN} = 0†
17	SUPPLY	I_+	Positive Supply Current	1.5	0.1	0.8	0.8	mA	V_{IN} = 5 V†
18	SUPPLY	I_-	Negative Supply Current	−5	−4	−3	−3	mA	V_{IN} = 5 V†
19	SUPPLY	I_L	Logic Supply Current	4.5	4.5	3.2	3.2	mA	V_{IN} = 5 V†
20	SUPPLY	I_R	Reference Supply Current	−2	−2	−2	−2	mA	Both V_{IN} = 5 V, V_{IN} = 0

†If driver has two channels, both are active.
*Typical values are to DESIGN AID ONLY, not guaranteed and not subject to production testing.
††Switch being tested ON or OFF as indicated. Input Logic Low 0.8 V.
Input Logic High 2V.

DG281	CMJB-NH
DG284	CMJA-NH
DG287	CMJC-NH
DG290	CMJB-NH

TRUTH TABLE

DEVICE	IN 1	SW 1	SW 3	IN 2	SW 2	SW 4
DG281	0.8 V	ON	–	0.8 V	ON	–
	2.0 V	OFF	–	2.0 V	OFF	–
DG284	0.8 V	OFF	OFF	0.8 V	OFF	OFF
	2.0 V	ON	ON	2.0 V	ON	ON
DG287	0.8 V	OFF	–	–	ON	–
	2.0 V	ON	–	–	OFF	–
DG290	0.8 V	OFF	ON	0.8 V	OFF	ON
	2.0 V	ON	OFF	2.0 V	ON	OFF

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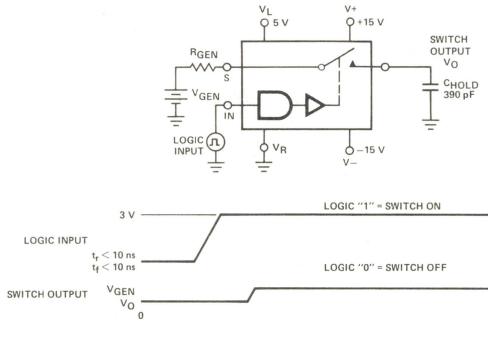
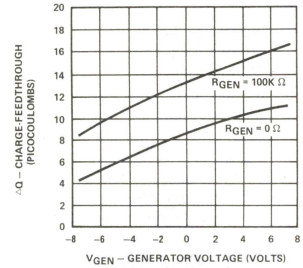
CHARGE INJECTION TEST CIRCUIT



Charge Feedthrough vs R_{GEN} and V_{GEN}

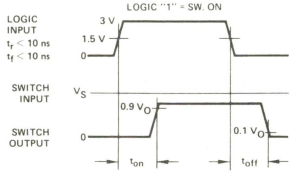


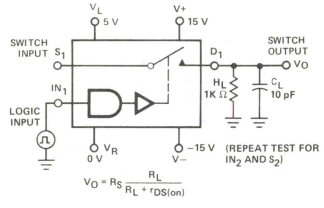
ΔV_O = ERROR VOLTAGE GENERATED ACROSS CAPACITOR

ΔQ = CHARGE INJECTED BY SWITCH DURING TURN-OFF $= \Delta V_O \times C_{HOLD}$

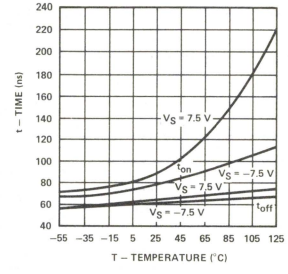
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



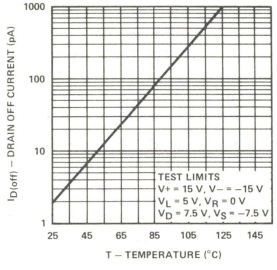


Switching Time vs V_S and Temperature

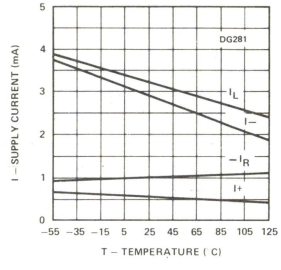


TYPICAL PERFORMANCE CURVES

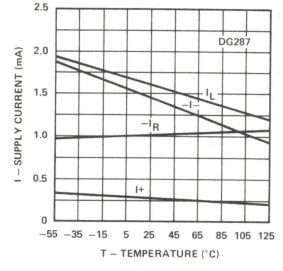
$I_{D(off)}$ vs. Temperature



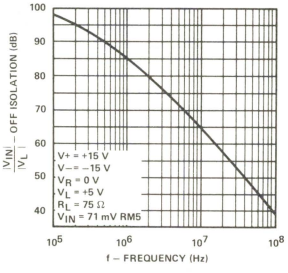
Supply Current vs Temperature



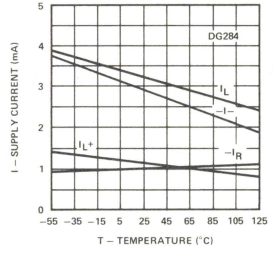
Supply Current vs Temperature



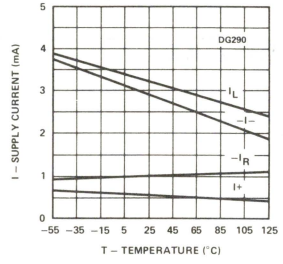
"OFF" Isolation vs Frequency



Supply Current vs Temperature



Supply Current vs Temperature



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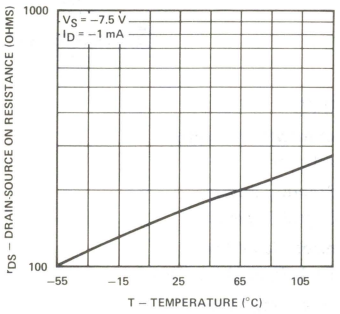
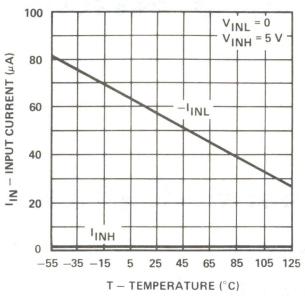
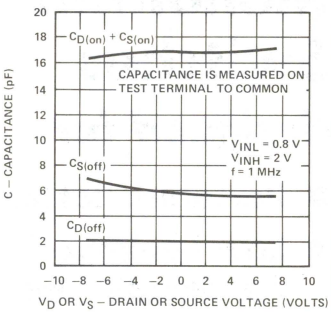
$r_{DS(on)}$ vs Temperature



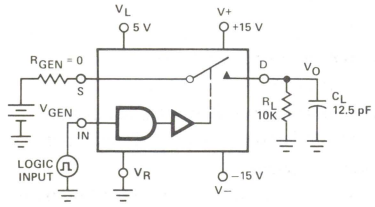
I_{IN} vs V_{IN} and Temperature



Capacitance vs V_D or V_S

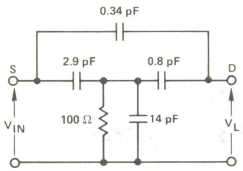


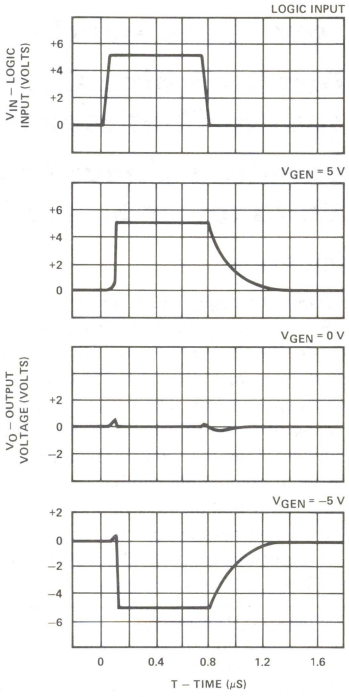
TYPICAL SWITCHING TRANSIENTS



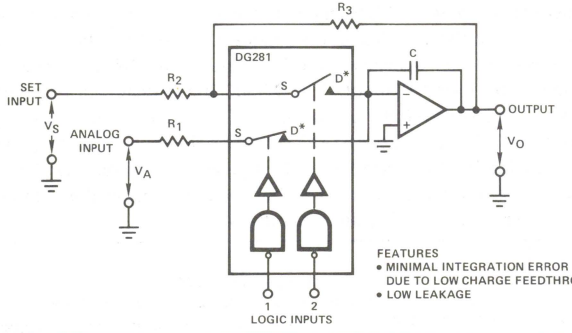
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall times.

Equivalent "OFF" Circuit



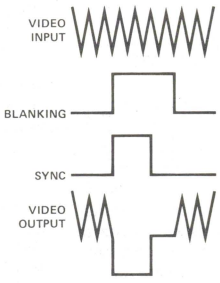


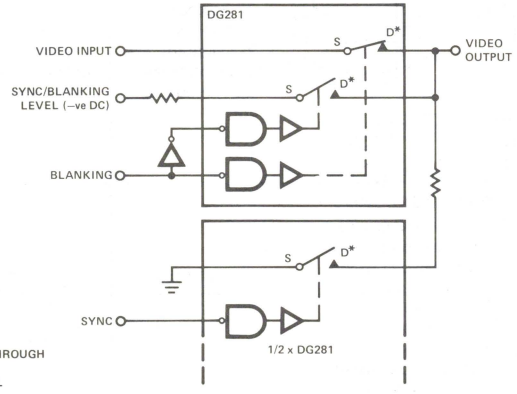
Application: THREE MODE INTEGRATOR



FEATURES
- MINIMAL INTEGRATION ERROR DUE TO LOW CHARGE FEEDTHROUGH
- LOW LEAKAGE

Application: VIDEO/BLANKING/SYNC. SIGNAL COMBINER





FEATURES
- MINIMAL OUTPUT SPIKES DUE TO LOW CHARGE FEEDTHROUGH
- NEGLIGIBLE FEEDTHROUGH DURING BLANKING INTERVAL

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DG300 DG301 DG302 DG303
DG304 DG305 DG306 DG307

Monolithic CMOS Analog Switches

Siliconix

designed for . . .

- **Portable, Battery Operated Circuits**
- **Low Leakage Switching i.e. Sample and Hold Circuits**
- **Communication Systems**
- **Low Level Switching Circuits**
- **Fast Switching Circuits such as Multiplexers**
- **Standard Linear Dual Supply Voltages or Single Supply Systems**

BENEFITS

- **Environmentally Rugged**
  - Latchproof CMOS
- **Low Standby Power**
  - 0.06 μW Typical
- **Minimizes Signal Error**
  - 0.1 nA Typical Leakage
- **Low Operating Power**
  - 0.06 μW Typical for DG304-407
- **Reduced Voltage Drop Across Switch in ON Condition**
  - $r_{ds(on)} < 50\ \Omega$
- **Minimizes Switching Time**
  - Typ t_{on} & $t_{off} < 180$ ns
- **Minimizes System Power Requirements**
  - Single Supply Operation Capabilities
- **Easily Interfaced**
  - TTL, DTL and CMOS Input Compatible
- **Reduces External Component Requirements**
  - Logic Input Overvoltage Protection

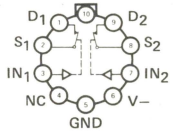
DESCRIPTION

The DG300 through DG307 switch family features four switching functions using CMOS technology for low and nearly constant ON resistance (less than 50 Ω) over the full analog signal range. In the ON condition the switches will conduct current in either direction with no offset voltage. With low power dissipation, (a few milliwatts for the DG300-303, a few hundred microwatts for the DG304-307), this series of switches becomes an ideal candidate for battery-powered or remote switching applications. The switching speed is among the fastest available with the low quiescent power dissipation. In the OFF condition, the switches will block voltages up to 30 V peak-to-peak. A logic input driver controls the ON/OFF state of the switches. (See the "Pin Configuration" for switch status with a logic "1" input.) The DG300-303 switches are TTL and CMOS input compatible and have a logic "0" state with an input less than 0.8 V and a logic "1" state with an input greater than 4.0 V. A pull-up resistor should be added for totem pole TTL outputs. The DG304-307 switches are CMOS input compatible and have a logic "0" state with an input less than 3.5 V and a logic "1" state with an input greater than 11 V (for 15 V positive supply). The logic inputs are protected against overvoltage up to 18 V above and 36 V below the positive supply. The combination of low cost, low power, low resistance and fast speed optimizes system design.

PIN CONFIGURATIONS

DUAL SPST DG300 or DG304

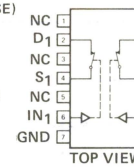
Metal Can Package
V+ (SUBSTRATE AND CASE)



TOP VIEW

ORDER NUMBERS:
DG300AA OR DG300BA
DG304AA OR DG304BA
SEE PACKAGE 2

Dual-In-Line and Flat Package



TOP VIEW

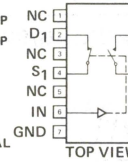
ORDER NUMBERS:
DG300AP OR DG300BP
DG304AP OR DG304BP
SEE PACKAGE 11
DG300CJ
DG304CJ
SEE PACKAGE 7
DG300AL OR DG304AL
SEE PACKAGE 16

LOGIC	SWITCH
0	OFF
1	ON

SPDT DG301 or DG305

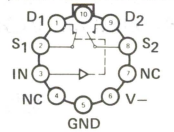
ORDER NUMBERS:
DG301AP OR DG301BP
DG305AP OR DG305BP
SEE PACKAGE 11
DG301CJ
DG305CJ
SEE PACKAGE 7
DG301AL OR DG305AL
SEE PACKAGE 16

Dual-In-Line and Flat Package



TOP VIEW

Metal Can Package
V+ (SUBSTRATE AND CASE)



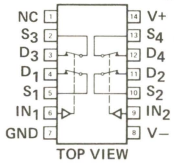
TOP VIEW

ORDER NUMBERS:
DG301AA OR DG301BA
DG305AA OR DG305BA
SEE PACKAGE 2

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

DUAL DPST DG302 or DG306

Dual-In-Line and Flat Package



TOP VIEW

ORDER NUMBERS:
DG302AP OR DG302BP
DG306AP OR DG306BP
SEE PACKAGE 11
DG302CJ
DG306CJ
SEE PACKAGE 7
DG302AL OR DG306AL
SEE PACKAGE 16

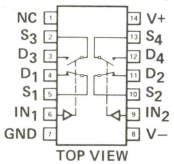
LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT DG303 or DG307

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ORDER NUMBERS:
DG303AP OR DG303BP
DG307AP OR DG307BP
SEE PACKAGE 11
DG303CJ
DG307CJ
SEE PACKAGE 7
DG303AL OR DG307AL
SEE PACKAGE 16

Dual-In-Line and Flat Package



TOP VIEW

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

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Siliconix

ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground . . . . . V^+ +18 V, V^+ −36 V
V_S or V_D . . . . . V^+ to V^-
V^+ to Ground . . . . . +36 V
V^+ to V^- . . . . . +36 V
Current, Any Terminal (Except S or D) . . . . 30 mA
Current, S or D, Continuous . . . . . 30 mA
Pulsed 1 ms 10% Duty Cycle . . . . . 100 mA
Operating Temperature (A Suffix) . . . −55 to +125°C
(B Suffix) . . . −20 to +85°C
(C Suffix) . . . . 0 to +70°C
Storage Temperature (A & B Suffix) . . −65 to +150°C
(C Suffix) . . . . −65 to +125°C

Power Dissipation*
14 Pin Sidebraze DIP (P)** . . . . . 825 mW
14 Pin Plastic DIP (J)*** . . . . . 470 mW
Metal Can (A)**** . . . . . 450 mW
Flat Package (L)***** . . . . . 750 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C
*****Derate 10 mW/°C above 75°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristics			Typ[1] 25°C	Max Limits A/B Suffix −55°C/−20°C	A/B Suffix 25°C	A/B Suffix 125°C/85°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Unit	Test Conditions V+ = +15 V, V− = −15 V, Gnd = 0 V	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability		±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance		30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = −10 mA	Note 2
3					30	50	50	75	50	50	75		V_D = −10 V, I_S = +10 mA	
4		$I_{S(off)}$	Source OFF Leakage Current		0.1		1	100		5	100	nA	V_S = +14 V, V_D = −14 V	Note 2
5					−0.1		−1	−100		−5	−100		V_S = −14V, V_D = +14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current		0.1		1	100		5	100		V_D = +14 V, V_S = −14 V	
7					−0.1		−1	−100		−5	−100		V_D = −14 V, V_S = +14 V	
8		$I_{D(on)}$	Channel ON Leakage Current		0.1		1	100		5	100		V_D = V_S = +14 V	Note 2
9					−0.1		−2	−200		−5	−200		V_D = V_S = −14 V	
10	INPUTS	I_{INH}	Input Current Input Voltage High	DG300-303 Only	−0.001	−1	−1	−1		−1		μA	V_{IN} = +15 V	
11				DG300-307 Only	0.001	1	1	1		1			V_{IN} = +15 V	
12		I_{INL}	Input Current Input Voltage Low		−0.001	−1	−1	−1		−1			V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn ON Time	DG300-303 Only	150		300					nS	See Switching Time Test Circuit	
14		t_{off}	Turn OFF Time		130		250							
15		t_{on}	Turn ON Time	DG304-307 Only	110		250							
16		t_{off}	Turn OFF Time		70		150							
17		$t_{on} - t_{off}$	Break-Before-Make Interval	DG301/303 DG305/307 Only	50								See Break-Before-Make Time Test Circuit	
18		$C_{S(off)}$	Source OFF Capacitance		14							pF	V_S = 0, Note 2	f = 1 MHz
19		$C_{D(off)}$	Drain OFF Capacitance		14								V_D = 0, Note 2	
20		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		40								V_D = V_S = 0, Note 2	
21		C_{IN}	Input Capacitance		6								V_{IN} = 0	
22					3.5								V_{IN} = +15 V	
23			OFF Isolation[3]		62							dB	V_{IN} = 0, R_L = 1K Ω, C_L = +15 pF V_S = 1 V_{RMS}, f = 500 kHz	
24	SUPPLY	I+	Positive Supply Current	DG300-303 Only	0.23	1	0.5	0.5		1		mA	V_{IN} = 4 V (One Input) (All Other Inputs = 0)	
25		I−	Negative Supply Current		−0.001	−10	−10	−100		−100		μA		
26		I+	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0.4 V (All Inputs)	
27		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				
28		I+	Positive Supply Current	DG304-307 Only	0.001	10	10	100		100			V_{IN} = +15 V (All Inputs)	
29		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				
30		I+	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0 (All Inputs)	
31		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				

NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = Input voltage to perform proper function, DG300-303: V_{IN} – For logic "1" = 4 V, for logic "0" = 0.8 V; DG304-307: V_{IN} – For logic "1" = 11 V, for logic "0" = 3.5 V
3. "OFF" Isolation ≙ 20 log V_S/V_D. V_S = Input to OFF switch, V_D = Output

DG300 ICMA-A DG302 ICMB-A
DG301 ICMA-B DG303 ICMB-B
DG304 ICMA-C DG306 ICMB-C
DG305 ICMA-D DG307 ICMB-D

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Monolithic CMOS Analog Switches

Siliconix

designed for . . .

- **Portable, Battery Operated Circuits**
- **Low Leakage Switching i.e. Sample and Hold Circuits**
- **Communication Systems**
- **Low Level Switching Circuits**
- **Fast Switching Circuits such as Multiplexers**
- **Standard Linear Dual Supply Voltages or Single Supply Systems**

BENEFITS

- **Environmentally Rugged**
  - Latchproof CMOS
- **Low Standby Power**
  - 0.06 μW Typical
- **Minimizes Signal Error**
  - 0.1 nA Typical Leakage
- **Low Operating Power**
  - 7.5 mW Typical
- **Reduced Voltage Drop Across Switch in ON Condition**
  - $r_{ds(on)} < 50\ \Omega$
- **Minimizes Switching Time**
  - Typ t_{on} & $t_{off} < 180$ ns
- **Minimizes System Power Requirements**
  - Single Supply Operation Capabilities
- **Easily Interfaced**
  - TTL, DTL / CMOS Input Compatible
  - Pin to Pin Replacement for DG180 Series Switches
- **Reduces External Component Requirements**
  - Logic Input Overvoltage Protection

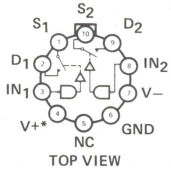
DESCRIPTION

The DG381 through DG390 switch family features four switching functions using CMOS technology for low and nearly constant ON resistance (less than 50 Ω) over the full analog signal range. In the ON condition the switches will conduct current in either direction with no offset voltage. With low power dissipation, a few milliwatts, this series of switches becomes an ideal candidate for battery-powered or remote switching applications. The switching speed is among the fastest available with the low quiescent power dissipation. In the OFF condition, the switches will block voltages up to 30 V peak-to-peak. A logic input driver controls the ON/OFF state of the switches. (See the "Pin Configuration" for switch status with a logic "1" input.) The switches are TTL and CMOS input compatible and have a logic "0" state with an input less than 0.8 V and a logic "1" state with an input greater than 4.0 V. A pull-up resistor should be added for totem pole TTL outputs. The logic inputs are protected against overvoltage up to 18 V above and 36 V below the positive supply. The combination of low cost, low power, low resistance and fast speed optimizes system design.

PIN CONFIGURATIONS

DUAL SPST DG381

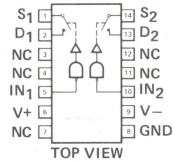
Metal Can Package



TOP VIEW

ORDER NUMBERS:
DG381AA OR DG381BA
SEE PACKAGE 2

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DG381AP OR DG381BP
SEE PACKAGE 11
DG381CJ
SEE PACKAGE 7

LOGIC	SW 1 SW 2
0	ON
1	OFF

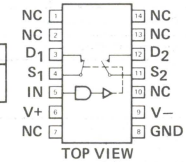
*(SUBSTRATE AND CASE)

SPDT DG387

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*(SUBSTRATE AND CASE)

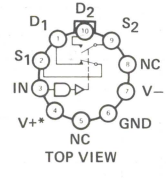
Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DG387AP OR DG387BP
SEE PACKAGE 11
DG387CJ
SEE PACKAGE 7

Metal Can Package



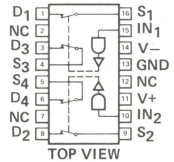
TOP VIEW

ORDER NUMBERS:
DG387AA OR DG387BA
SEE PACKAGE 2

DUAL DPST DG384

ORDER NUMBERS:
DG384AP OR DG384BP
SEE PACKAGE 12
DG384CJ
SEE PACKAGE 8

Dual-In-Line Package



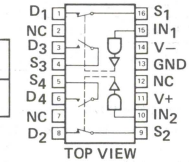
TOP VIEW

LOGIC	SW 1–4
0	OFF
1	ON

DUAL SPDT DG390

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Dual-In-Line-Package



TOP VIEW

ORDER NUMBERS:
DG390AP OR DG390BP
SEE PACKAGE 12
DG390CJ
SEE PACKAGE 8

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

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ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground . . . . . V+ +18 V, V+ −36 V
V_S to V_D . . . . . V+, V−
V+ to Ground . . . . . +36 V
V+ to V− . . . . . +36 V
Current, Any Terminal (Except S or D) . . . . 30 mA
Current, S or D, Continuous . . . . . 30 mA
Pulsed 1 ms 10% Duty Cycle . . . . . 100 mA
Operating Temperature (A Suffix) . . −55°C to +125°C
(B Suffix) . . −20°C to +85°C
(C Suffix) . . . 0°C to +70°C
Storage Temperature (A & B Suffix) . . −65°C to +150°C
(C Suffix) . . . . −65°C to +125°C

Power Dissipation*
14 Pin Sidebraze DIP (P)** . . . . . 825 mW
14 Pin Plastic DIP (J)*** . . . . . 470 mW
Metal Can (A)**** . . . . . 450 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristics		Typ[1] 25°C	Max Limits A/B Suffix −55°C/−20°C	Max Limits A/B Suffix 25°C	Max Limits A/B Suffix 125°C/85°C	Max Limits C Suffix 0°C	Max Limits C Suffix 25°C	Max Limits C Suffix 70°C	Unit	Test Conditions V+ = +15 V, V− = −15 V, Gnd = 0 V	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = −10 mA	Note 2
3				30	50	50	75	50	50	75		V_D = −10 V, I_S = +10 mA	
4		$I_{S(off)}$	Source OFF Leakage Current	0.1		1	100		5	100	nA	V_S = +14 V, V_D = −14 V	Note 2
5				−0.1		−1	−100		−5	−100		V_S = −14 V, V_D = +14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.1		1	100		5	100		V_D = +14 V, V_S = −14 V	
7				−0.1		−1	−100		−5	−100		V_D = −14 V, V_S = + 14 V	
8		$I_{D(on)}$	Channel ON Leakage Current	0.1		1	100		5	100		V_D = V_S = +14 V	Note 2
9				−0.1		−2	−200		−5	−200		V_D = V_S = −14 V	
10	IN	I_{INH}	Input Current Input Voltage High	−0.001	−1	−1	−1		−1		μA	V_{IN} = +5 V	
11				0.001	1	1	1		1			V_{IN} = +15 V	
12		I_{INL}	Input Current Input Voltage Low	−0.001	−1	−1	−1		−1			V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn ON Time	150		300					nS	See Switching Time Test Circuit	
14		t_{off}	Turn OFF Time	130		250							
15		$t_{on} - t_{off}$	Break-Before-Make Interval DG387/390 only	50								See Break-Before-Make Time Test Circuit	
16		$C_{S(off)}$	Source OFF Capacitance	14							pF	V_S = 0, Note 2	f = 1 MHz
17		$C_{D(off)}$	Drain OFF Capacitance	14								V_D = 0, Note 2	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	40								V_D = V_S = 0, Note 2	
19		C_{IN}	Input Capacitance	6								V_{IN} = 0	
20				3.5								V_{IN} = +15 V	
21			OFF Isolation[3]	62							dB	V_{IN} = 0, R_L = 1K Ω, C_L = +15 pF V_S = 1 V_{RMS}, f = 500 kHz	
22	SUPPLY	I+	Positive Supply Current	0.23	1	0.5	0.5		1		mA	V_{IN} = 4 V (One Input) (All Other Inputs = 0)	
23		I−	Negative Supply Current	−0.001	−10	−10	−100		−100				
24		I+	Positive Supply Current	0.001	10	10	100		100		μA	V_{IN} = 0.4 V (All Inputs)	
25		I−	Negative Supply Current	−0.001	−10	−10	−100		−100				

NOTES:

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing
2. V_{IN} = Input voltage to perform proper function, V_{IN} for logic "1" = 4 V, for logic "0" = 0.8 V
3. "OFF" Isolation $\triangleq$ 20 log V_S/V_D = Input to OFF switch, V_D = Output

DG381 ICMA-E DG384 ICMB A
DG387 ICMA B DG390 ICMB B

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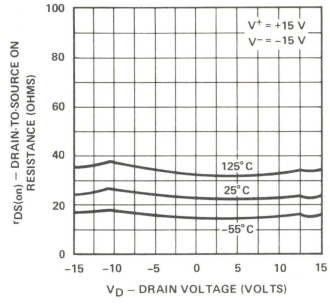
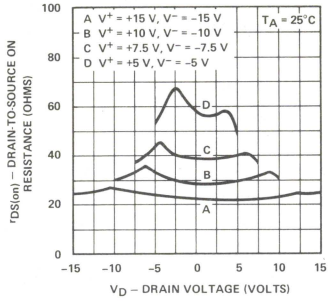
TYPICAL CHARACTERISTICS

$r_{DS(on)}$ vs V_D and Temperature

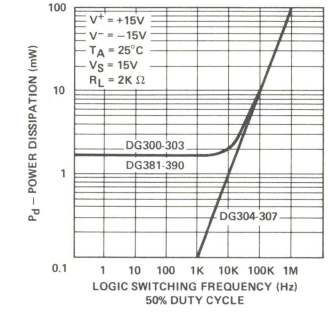


$r_{DS(on)}$ vs V_D and Power Supply Voltage

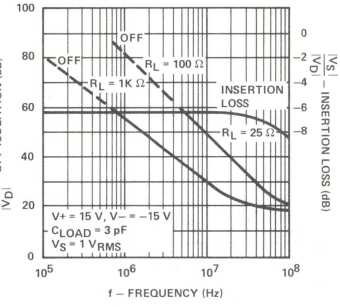


Device Power Dissipation vs Switching Frequency

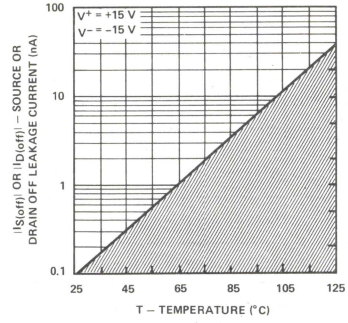
Single Logic Input



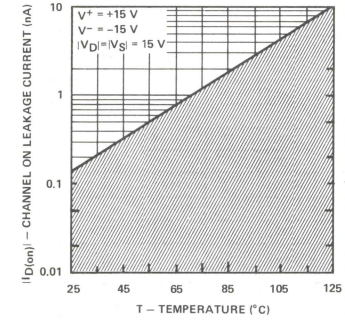
OFF Isolation Insertion Loss vs Frequency



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*

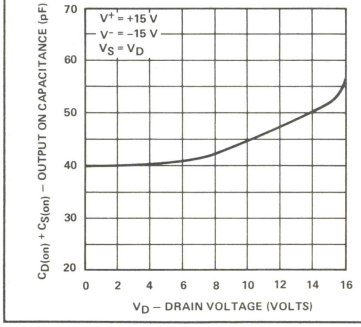


$I_{D(on)}$ vs Temperature*

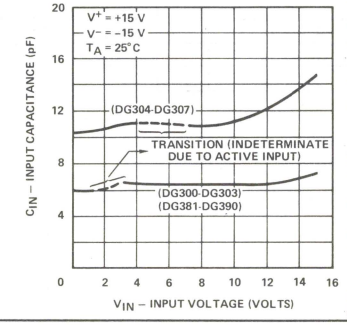


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

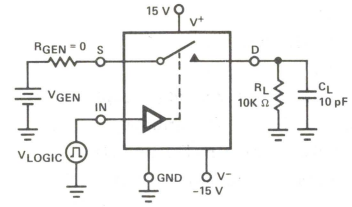
Output ON Capacitance vs Drain Voltage



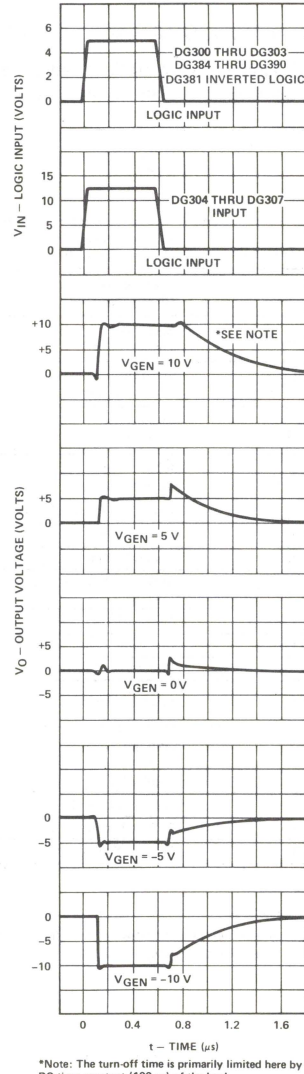
Input Capacitance vs Input Voltage



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.



*Note: The turn-off time is primarily limited here by the RC time constant (100 ns) of the load.

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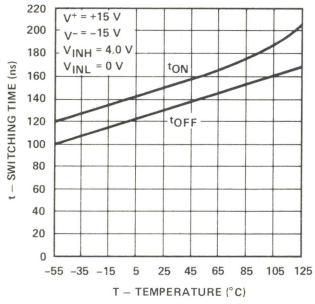
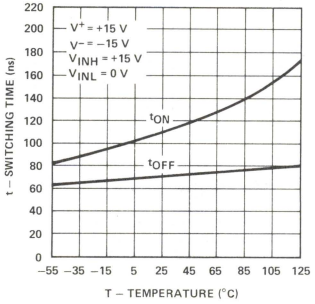
TYPICAL CHARACTERISTICS (Cont'd)

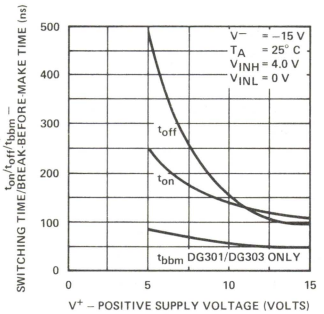
Switching Time vs Temperature
DG300-303, DG381-390



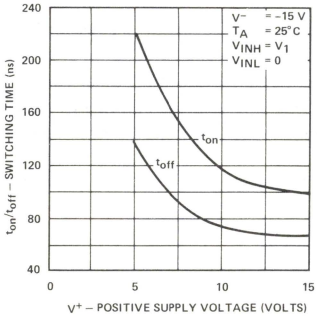
Switching Time vs Temperature
DG304-307



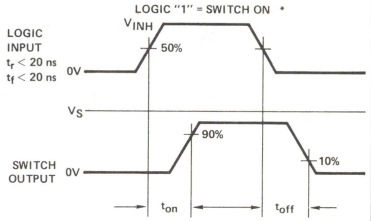
Switching Time and Break-Before-Make Time vs Positive Supply Voltage
DG300-303, DG381-390



Switching Time vs Positive Supply Voltage
DG304-307

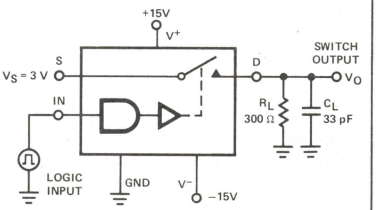


SWITCHING TIME TEST CIRCUIT (DG300-307 DG381-390)

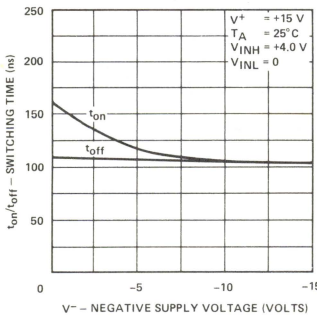


		VINH
DG300-303	DG381-DG390	4 V
DG304-307		15 V

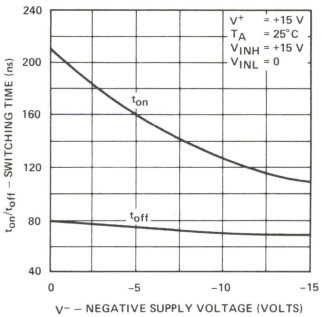
*INVERTED LOGIC FOR DG381



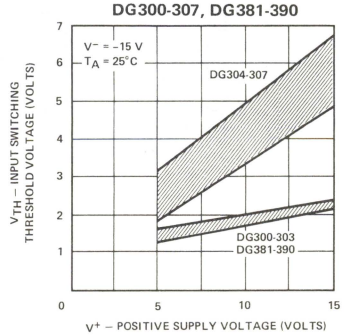
Switching Time vs Negative Supply Voltage
DG300-303, DG381-390



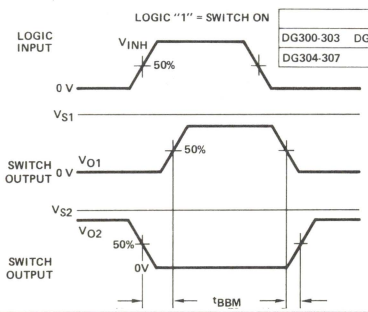
Switching Time vs Negative Supply Voltage
DG304-307



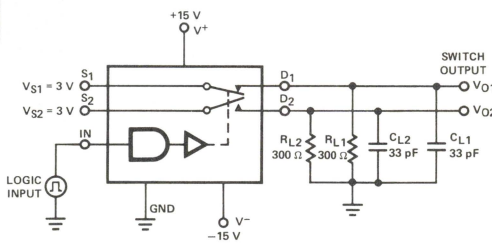
Input Switching Threshold vs Positive Supply Voltage
DG300-307, DG381-390



BREAK-BEFORE-MAKE TIME TEST CIRCUIT SPDT (DG301, DG303, DG305, DG307, DG384, DG390)



		VINH
DG300-303	DG381-DG390	4 V
DG304-307		15 V



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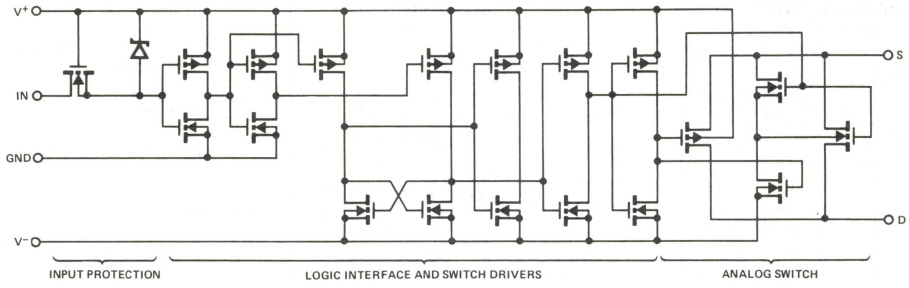
PARTIAL SCHEMATIC OF TYPICAL SWITCH (DG300-307, DG381-390)

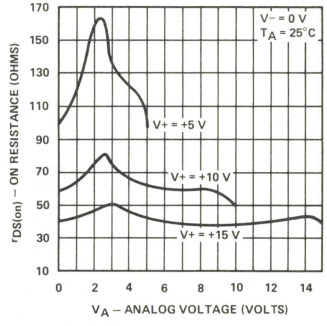


APPLICATIONS

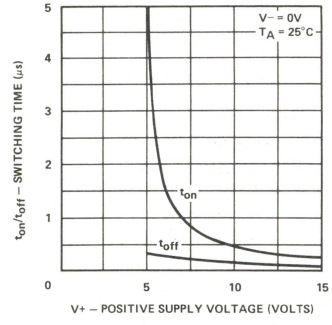
Single Supply Operation

The DG300 series of analog switches will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased $r_{DS(ON)}$; 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied in the Figures below. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 volts.

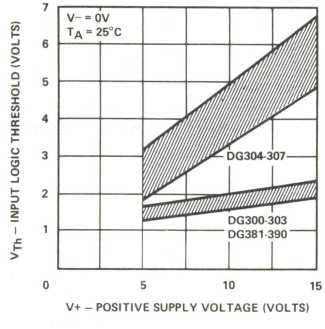
$R_{DS(on)}$ vs Analog and Positive Supply Voltage With V− = 0V



Switching Time vs V+ — Positive Supply Voltage



Input Threshold Voltage vs Positive Supply



Single Supply Range:
(V− and GND Tied Together)
V+: +5 V to +25 V

Analog Signal Range:
$V- \leq V_{ANALOG} \leq V+$

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Quad Monolithic SPST CMOS Analog Switch *designed for...*

Siliconix

ADVANCE INFORMATION

- **Portable, Battery Instrumentation**
- **Automotive Applications**
- **Computer Peripherals**
- **High Speed Multiplexing**
- **Low Leakage Switching**
- **Sample and Hold**
- **Data Acquisition Systems**

BENEFITS

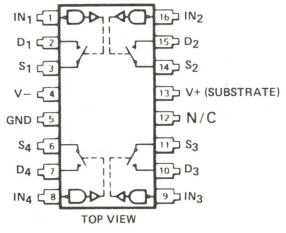
- **High Speed Switching With Break-Before-Make**
  - t_{on} = 100 nsec Typical
  - t_{off} = 80 nsec Typical
- **Single Supply Operations**
  - +5 V to +30 V
- **CMOS Compatible (positive logic)**
- **Wide Signal Range ±15 V**
- **Low Standby Power**
  - 300 μWatt Max
- **Minimizes Signal Error**
  - $r_{DS} < 100\ \Omega$
  - $I_{D(off)}$ = 0.1 nA Typical
- **Environmentally Rugged**
  - Latchproof CMOS Process

DESCRIPTION

The DG308 is a monolithic quad single-pole single-throw analog switch fabricated in complementary MOS technology. In the ON condition, each switch will conduct current in either direction and in the OFF condition each switch will block voltages up to 30 volts peak-to-peak. The ON-OFF state of each switch is controlled by a driver. With CMOS logic '1' at the input the switch will be ON, with logic '0' at the input the switch will be OFF.

PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

LOGIC	SWITCH
0	OFF
1	ON

TENTATIVE DATA SHEET

This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.

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ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground . . . . . V^+ +18 V, V^+ −36 V
V_S or V_D . . . . . V^+ to V^-
V^+ to Ground . . . . . +36 V
V^+ to V^- . . . . . +36 V
Current, Any Terminal (Except S or D) . . . . . 30 mA
Current, S or D, Continuous . . . . . 30 mA
Pulsed 1 ms 10% Duty Cycle . . . . . 100 mA
Operating Temperature (A Suffix) . . . . . −55 to +125°C
(B Suffix) . . . . . −20 to +85°C
(C Suffix) . . . . . 0 to +70°C
Storage Temperature (A & B Suffix) . . . . −65 to +150°C
(C Suffix) . . . . . −65 to +125°C
Power Dissipation (Package)*
16 Pin DIP** . . . . . 900 mW
16 Pin Plastic DIP*** . . . . . 470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 12 mW/°C above 75°C.

***Derate 6.5 mW/°C above 25°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		(Note 1) TYP 25°C	MAX LIMITS A/B SUFFIX −55°C −20°C	A/B SUFFIX 25°C	A/B SUFFIX 125°C/ 85°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS V+ = +15 V V− = −15 V, Gnd = 0 V	
1	SWITCH	V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	<90		100			100		Ω	V_D = 10 V, I_S = −1 mA	V_{IN} = 15 V
3	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	<90		100			100		Ω	V_D = −10 V, I_S = 1 mA	V_{IN} = 15 V
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	0.1		1			5		nA	V_S = 14 V, V_D = −14 V	V_{IN} = 0 V
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	−0.1		−1			−5		nA	V_S = −14 V, V_D = 14 V	V_{IN} = 0 V
6	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	0.1		1			5		nA	V_S = 14 V, V_D = −14 V	V_{IN} = 0 V
7	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	−0.1		−1			−5		nA	V_S = −14 V, V_D = 14 V	V_{IN} = 0 V
8	SWITCH	$I_{D(on)}$	Drain ON Leakage Current	0.1		1			5		nA	V_D = V_S = 14 V	V_{IN} = 15 V
9	SWITCH	$I_{D(on)}$	Drain ON Leakage Current	−0.1		−2			−5		nA	V_D = V_S = −14 V	V_{IN} = 15 V
10	INPUT	I_{INH}	Input Current Input Voltage High	0.001		1			1		μA	V_{IN} = 15 V	
11	INPUT	I_{INL}	Input Current Input Voltage Low	−0.001		−1			−1		μA	V_{IN} = 0 V	
12	DYNAMIC	t_{on}	Turn-ON Time	100		170			170		ns	R_L = 1K Ω	
13	DYNAMIC	t_{off1}	Turn-OFF Time	70		95			95		ns	R_L = 1K Ω	
14	DYNAMIC	t_{off2}	Turn-OFF Time	95							ns	See Switching Time Test Circuit C_L = 35 pF, V_S = 3 V	
15	DYNAMIC	$C_{S(off)}$	Source OFF	7							pF	V_S = 0 V, V_{IN} = 0 V	
16	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	7							pF	V_D = 0 V, V_{IN} = 0 V	
17	DYNAMIC	$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	20							pF	V_D = V_S = 0 V, V_{IN} = 15 V	
18		OFF Isolation (Note 2)		>50							dB	V_{IN} = 0 V, R_L = 1K Ω, C_L = 15 pF V_S = 1 V_{rms}, f = 1 MHz	
19	SUP	I_+	Positive Supply Current			10			100		μA	V_{IN} = 15 V or 0 V	
20	SUP	I_-	Negative Supply Current			−10			−100		μA	V_{IN} = 15 V or 0 V	

NOTES:

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. OFF Isolation = $20 \log_{10} \frac{|V_D|}{|V_S|}$ V_S = Input to OFF Switch, V_D = Output

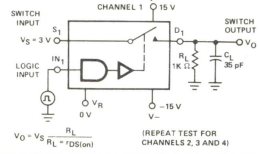
TENTATIVE DATA SHEET

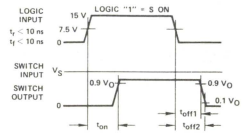
ICMD

This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = CONSTANT with logic input waveform as shown. Note that V_S may be positive or negative as per switching time test circuit. V_O is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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8-Channel Multiplex Switch with Decode

Siliconix

designed for . . .

- **Multiplexing Signals**
- **Data Acquisition**

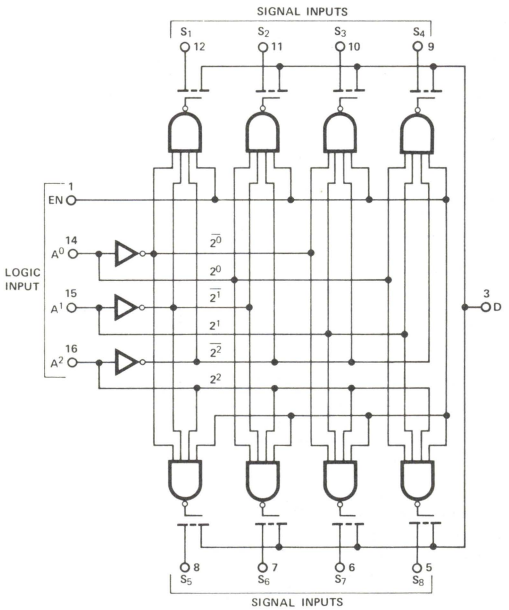
BENEFITS

- **Reduces Cross-Talk in Systems**
  - Break-Before-Make Switching
- **Easily Interfaced**
  - Pull-Up Resistors on Inputs for TTL Compatibility

DESCRIPTION

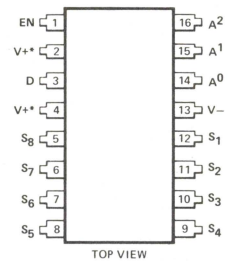
The DG501 is designed to function as a single-pole, 8-position (plus OFF) electronic switch. The function is implemented by using eight P-channel MOS field-effect transistors as analog switches. In the ON state, each switch will conduct current equally well in either direction and in the OFF state each switch will block voltages up to 10 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word plus an Enable-Inhibit input. The truth table shown below indicates the binary word required to select any one of the eight switch positions. Logic input levels "L" and "H" correspond to positive logic "0" and "1". Assuming supply voltages of +5 V and −20 V, logic "L" $\leq$ 0.6 V and logic "H" $\geq$ 3.5 V. "Pull-up" resistors are provided at each logic input to improve TTL compatibility. The rise and fall times of the drivers are designed to provide break-before-make switch action.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



ORDER NUMBERS: DG501AP OR DG501BP
SEE PACKAGE 12

DG501CJ
SEE PACKAGE 8

*Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

TRUTH TABLE

LOGIC INPUTS				CHANNEL
A^0	A^1	A^2	En	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

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ABSOLUTE MAXIMUM RATINGS

V+ to V− . . . . . −0.3, +30 V
V+ to V_A, V_{En} . . . . . −0.3, +30 V
V+ to V_D or V_S . . . . . −0.3, +30 V
V_D to V_S . . . . . ±25 V
V_A, V_{En} to V− . . . . . 30 V
V_D or V_S to V− . . . . . 30 V
Current (Any Terminal) . . . . . −20 mA
Storage Temperature (A & B Suffix) . . . . . −65 to 150°C
(C Suffix) . . . . . −65 to 125°C
Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
(C Suffix) . . . . . 0 to 70°C
Power Dissipation*
16 Pin DIP** . . . . . 900 mW
16 Pin Plastic DIP*** . . . . . 470 mW

*Device mounted with all leads welded or soldered to PC board.

**Derate 12 mW/°C above 75°C

***Derate 6.5 mW/°C above 25°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS DG501A −55°C	DG501A 25°C	DG501A 125°C	DG501B/C −20°C/0°C	DG501B/C 25°C	DG501B/C 85°C/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V− = −20 V, V+ = 5 V, V_{EN} = 3.5 V, V_{AL} = 0.6 V, V_{AH} = 3.5 V	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	225	150	150	200	Ω	V_D = 5 V	I_S = −1 mA, V− = −20 V
2				200	200	300	200	200	300		V_D = 0	
3				250	250	375	250	250	350		V_D = −5 V	
4				200	200	300	200	200	300		V_D = 5 V	I_S = −100 μA, V− = −15 V
5				250	250	375	250	250	350		V_D = 0	
6				600	600	900	600	800	900		V_D = −5 V	
7		$I_{S(off)}$	Source OFF Leakage Current		−1	−1000		−3	−150	nA	V_S = −5 V, V_D = 5 V	V_{EN} = 0.6 V
8		$I_{D(off)}$	Drain OFF Leakage Current		−8	−4000		−10	−500		V_D = −5 V, V_S = 5 V	
9		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		8	4000		10	500		V_D = V_S = 5 V	
10	IN	I_{INL}	Input Current, Input Voltage Low		−1.2			−1.2		mA	V_{AL} = 0	
11		I_{INH}	Input Current, Input Current High		−150 Min			−150 Min		μA	V_{AH} = 3.5 V	
12	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer		1.5			1.5		μs	V− = −20 V	See Switching Time Test Cricuit V_{S1} = ±1 V, V_{S8} = +1 V, V_{S2-7} = gnd
13					2.5			2.5			V− = −15 V	
14		t_{on}	Turn-ON Time		1.2 Typ*			1.2 Typ*			See Switching Time Test Circuit $V_{S(all)}$ = 1 V	
15		t_{off}	Turn-OFF Time		0.8 Typ*			0.8 Typ*				
16		t_{open}	Break-Before-Make Interval		0.05 Typ*			0.05 Typ*				
17		t_{on}	Turn-ON Time		2.0 Typ*			2.0 Typ*			Same as Above, Except V− = −15 V	
18		t_{off}	Turn-OFF Time		0.8 Typ*			0.8 Typ*				
19		$C_{S(off)}$	Source OFF Capacitance		10 Typ*			10 Typ*		pF	V_S = V_D = 5 V	V_{EN} = 0.6 V, f = 1 MHz
20		$C_{D(off)}$	Drain OFF Capacitance		20 Typ*			20 Typ*				
21	SUPPLY	I−	Drain Supply Current		−6			−6		mA	V_{EN} = 0	All V_A = 0
22		I+	Source Supply Current		8			8				
23		I−	Drain Supply Current		−6			−6			V_{EN} = 3.5 V	
24		I+	Source Supply Current		7			7				

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

IPAA

APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{EN} Enable Input Voltage Min High/ Max Low (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Signal Range (V)
+5**	−20	3.5/0.6	3.5/0.6	−5 to +5
+5	−15	3.5/0.6	3.5/0.6	−5 to +5

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical parameters chart based on V+ = 5 V, V− = −20 V.

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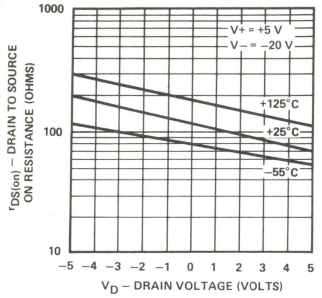
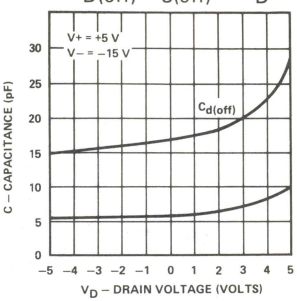
TYPICAL CHARACTERISTICS

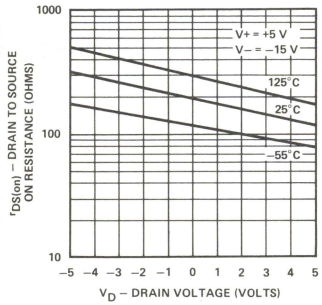
$r_{DS(on)}$ vs V_D and Temperature



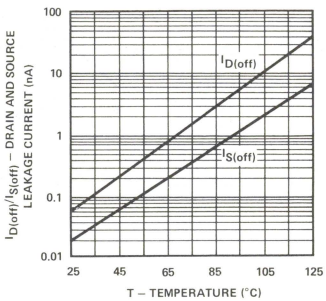
$C_{D(off)}$, $C_{S(off)}$ vs V_D



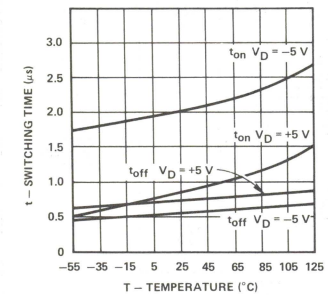
$r_{DS(on)}$ vs V_D and Temperature



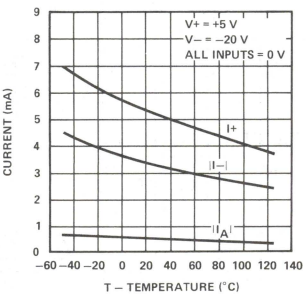
$I_{D(off)}/I_{S(off)}$ vs Temperature



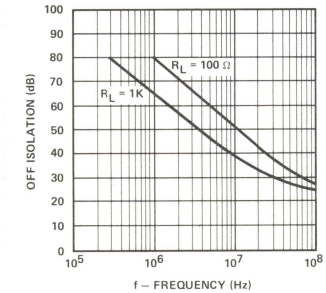
Switching Time vs Temperature

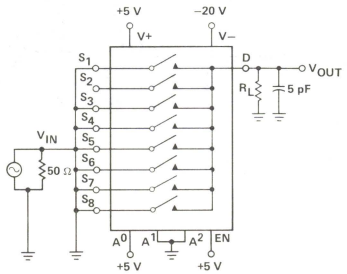


Supply Current vs Temperature

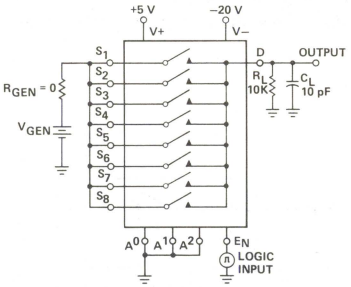


"OFF" Isolation vs R_L and Frequency

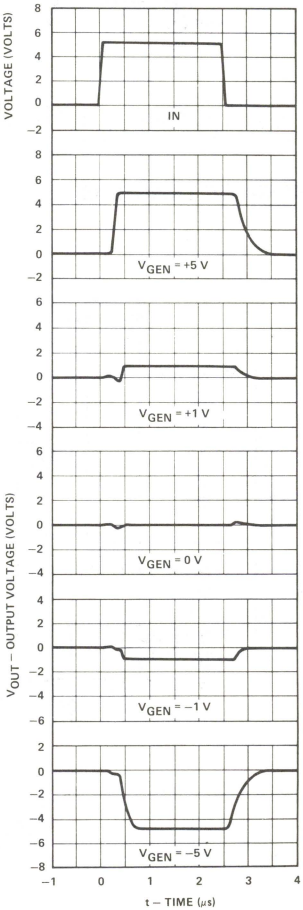




"OFF" ISOLATION = 20 LOG $\frac{|V_{OUT}|}{|V_{IN}|}$



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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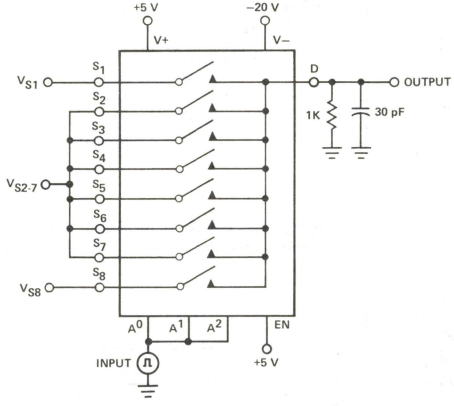
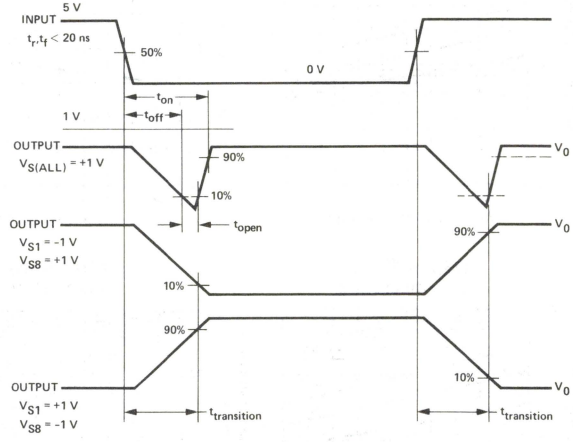
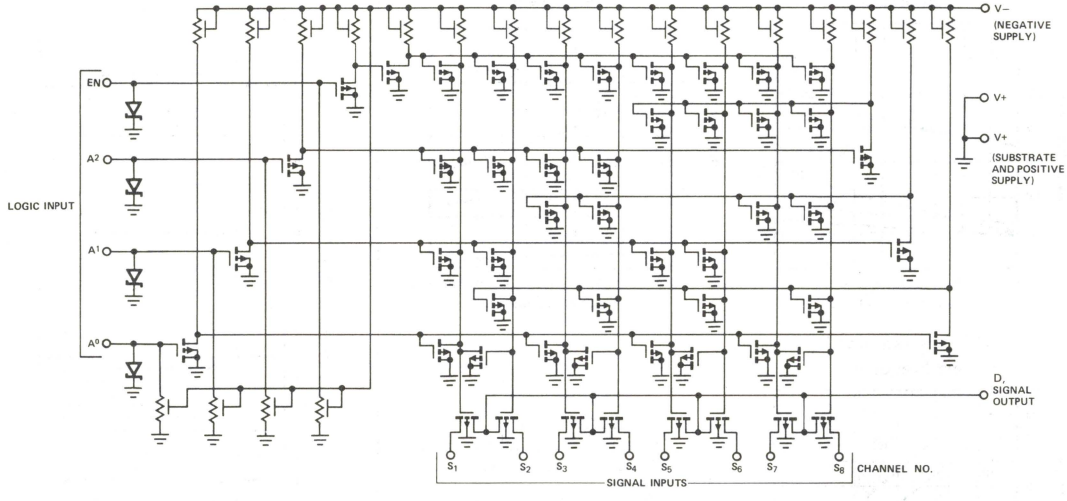
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





SCHEMATIC DIAGRAM



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8-Channel Multiplex Switch with Decode

Siliconix

designed for . . .

- **Multiplexing Signals**
- **Data Acquisition**

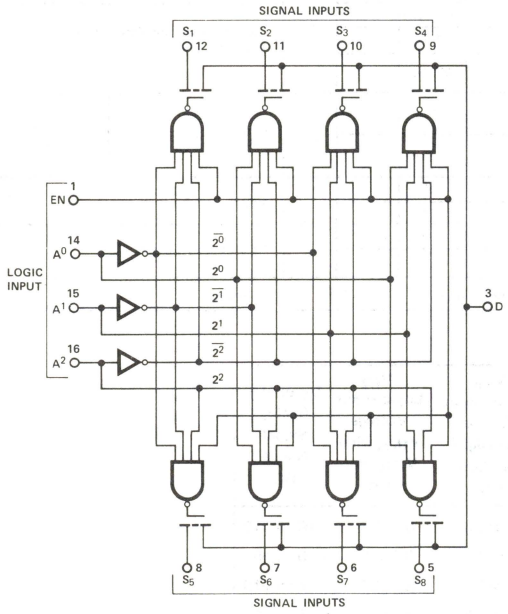
BENEFITS

- **Reduces Cross-Talk in Systems**
  - Break-Before-Make Switching

DESCRIPTION

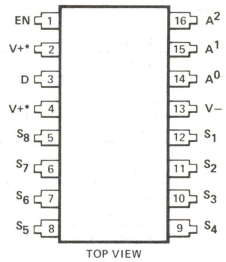
The DG503 is designed to function as a single-pole, 8-position (plus OFF) electronic switch. The function is implemented by using eight P-channel MOS field-effect transistors as analog switches. In the ON state, each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word plus an Enable-Inhibit input. The truth table shown below indicates the binary word required to select any one of the eight switch positions. Logic input levels "L" and "H" correspond to positive logic "0" and "1". Assuming supply voltages of 10 and −20 V, logic "L" $\leq$ 0.6 V and logic "H" $\geq$ 8.5 V. The rise and fall times of the drivers are designed to provide break-before-make switch action.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Dual In-Line Package



ORDER NUMBERS: DG503AP OR DG503BP
SEE PACKAGE 12

*Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

TRUTH TABLE

LOGIC INPUTS				CHANNEL
A^0	A^1	A^2	En	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

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ABSOLUTE MAXIMUM RATINGS

V+ to V− . . . . . −0.3, 33 V
V+ to V_A, V_{En} . . . . . −0.3, 33 V
V+ to V_D or V_S . . . . . −0.3, 33 V
V_D to V_S . . . . . ±25 V
V_A, V_{En} to V− . . . . . 33 V
V_D or V_S to V− . . . . . 33 V

Current (Any Terminal) . . . . . −20 mA
Storage Temperature (A & B Suffix) . . . . . −65 to 150°C
Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
Power Dissipation* . . . . . 900 mW

*All leads soldered or welded to PC board. Derate 12 mW/°C above 75°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	25°C	125°C	MAX LIMITS B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V− = −20 V, V+ = 10 V, V_{En} = 8.5 V, V_{AL} = 0.6 V, V_{AH} = 8.5 V	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	225	150	150	200	Ω	V_D = 10 V	I_S = −1 mA
2				250	250	375	250	250	350		V_D = 0	
3				600	800	1250	600	800	1000		V_D = −10 V	I_S = −100 µA
4		$I_{S(off)}$	Source OFF Leakage Current		−2	−2000		−3	−150	nA	V_S = −10 V, V_D = 10 V	V_{En} = 0.6 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−8	−4000		−10	−500		V_D = −10 V, V_S = 10 V	
6		$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		8	4000		10	500		$V_D = V_S$ = 10 V	
7	IN	I_{INL}	Input Current, Input Voltage Low		−1			−1		µA	V_{AL} = 0	
8	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer		1.5			1.5		µs	See Switching Time Test Circuit V_{S1} = ±1 V, V_{S8} = ∓1 V, V_{S2-7} = gnd	
9		t_{on}	Turn-ON Time		1.2 Typ*			1.2 Typ*			See Switching Time Test Circuit $V_{S(all)}$ = ±1 V	
10		t_{off}	Turn-OFF Time		0.8 Typ*			0.8 Typ*				
11		t_{open}	Break-Before-Make Interval		0.05 Typ*			0.05 Typ*				
12		$C_{S(off)}$	Source OFF Capacitance		5 Typ*			5 Typ*		pF	$V_S = V_D$ = 0	V_{En} = 0.5 V, f = 1 MHz
13		$C_{D(off)}$	Drain OFF Capacitance		20 Typ*			20 Typ*				
14	SUPPLY	I−	Drain Supply Current		−6			−6		mA	V_{En} = 0	
15		I+	Source Supply Current		8			8				
16		I−	Drain Supply Current		−6			−6			V_{En} = 8.5 V, V_A = 0	
17		I+	Source Supply Current		7			7				

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

IPAA

APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{En} Enable Input Voltage Min High/ Max Low (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Signal Range (V)
+10**	−20	8.5/0.6	8.5/0.6	−10 to +10
+5	−20	3.5/0.6	3.5/0.6	−10 to +5
+10	−15	8.5/0.6	8.5/0.6	−5 to +10
+5	−15	3.5/0.6	3.5/0.6	−5 to +5

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical parameters chart based on V+ = +10 V, V− = −20 V.

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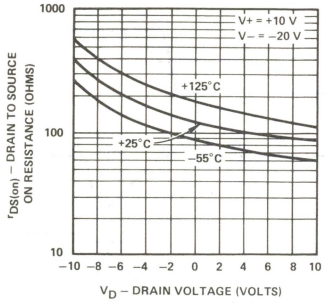
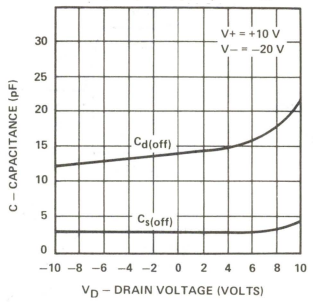
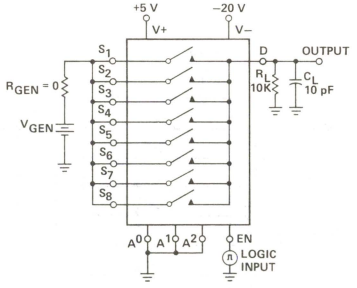
TYPICAL CHARACTERISTICS

$r_{DS(on)}$ vs V_D and Temperature



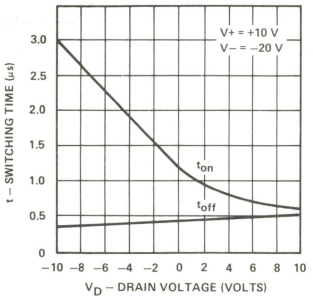
$C_{D(off)}$, $C_{S(off)}$ vs V_D



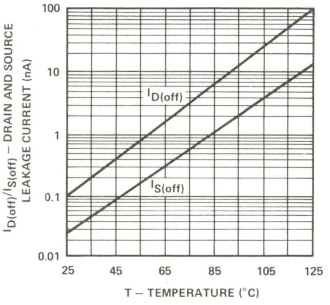


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

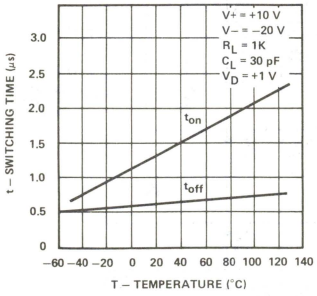
Switching Time vs V_D



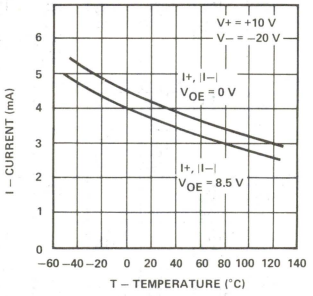
$I_{D(off)}/I_{S(off)}$ vs Temperature



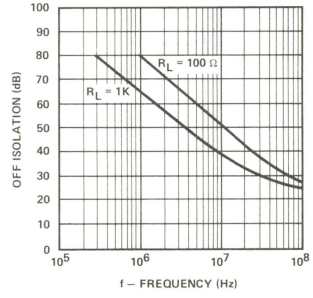
Switching Time vs Temperature

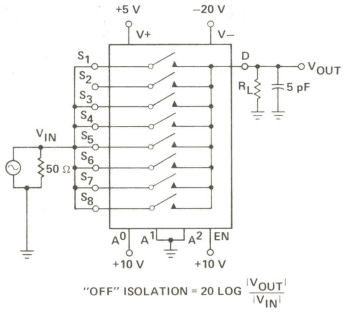


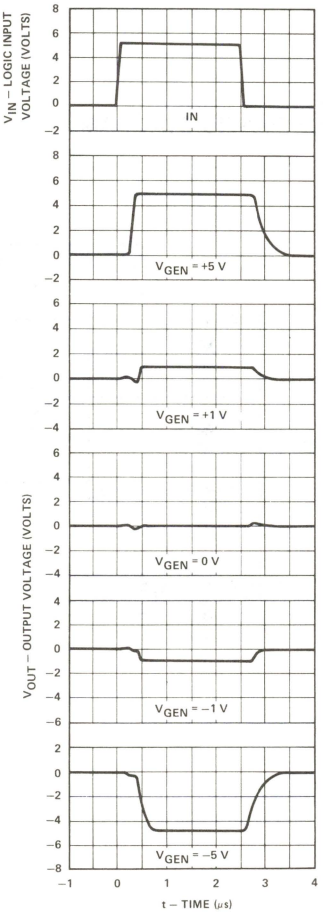
Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency







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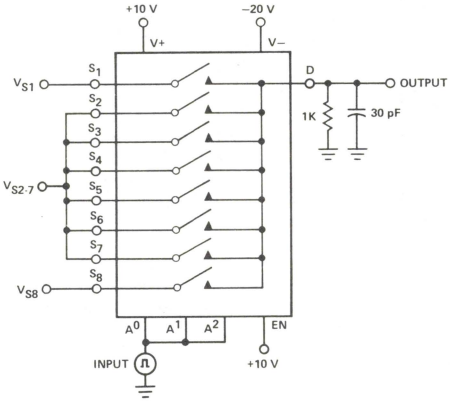
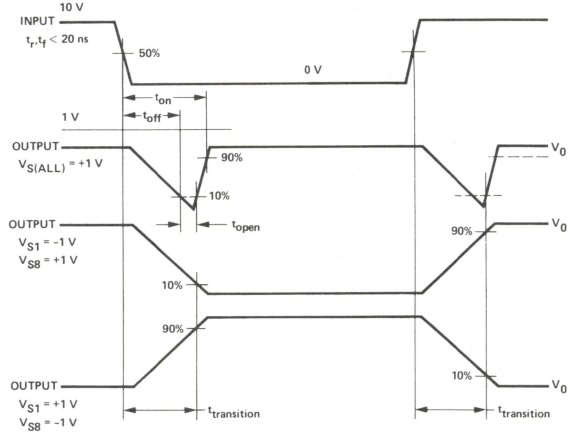
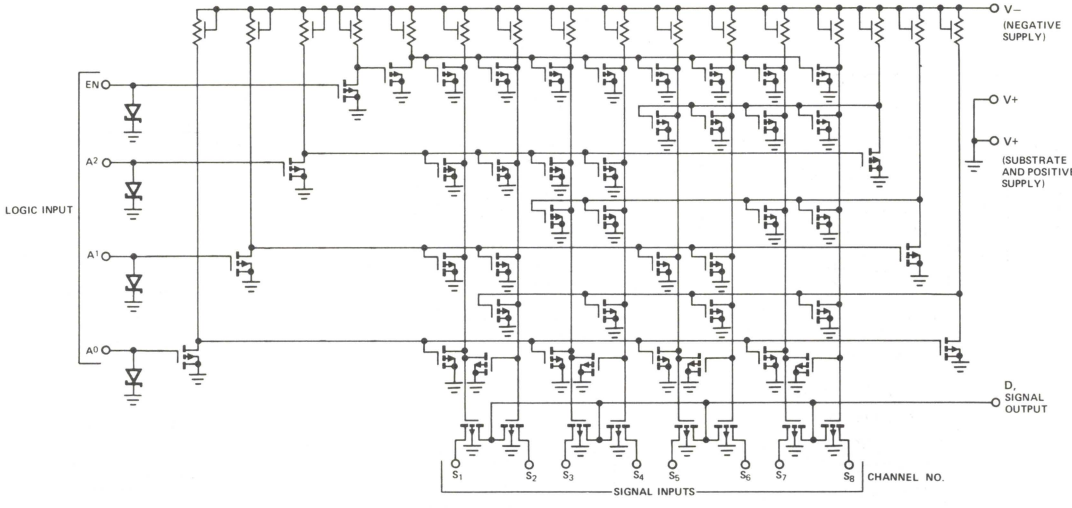
SWITCHING TIME TEST CIRCUIT





SCHEMATIC DIAGRAM



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Differential 8-Channel/ 16-Channel CMOS Analog Multiplexer *designed for...*

- **Data Acquisition Systems**
- **Multiplexing Reference Signals**
- **Communication Systems**

BENEFITS

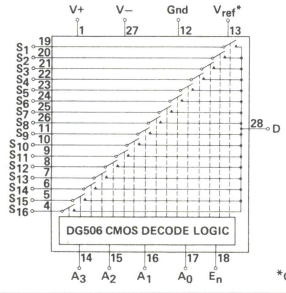
- **Environmentally Rugged**
  - Latchproof CMOS
- **Easily Interfaced**
  - TTL, DTL and CMOS Direct Control Over Military Temperature Range
- **Low Stand-By Power**
  - 36 mW Typical Stand-By Power
- **Reduces System Cross-Talk**
  - Break-Before-Make Switching Action
- **Reduces External Component Requirements**
  - ±15 V Analog Signal Range with ±15 V Supplies

DESCRIPTION

The DG506 is a single-pole 16-position (plus OFF) electronic switch array [DG507 is a double-pole 8-position (plus OFF)] which employs 16 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction, and in the OFF condition each switch will block voltages up to 30 volts peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 4-bit binary word (DG507 by a 3-bit binary word) input plus an Enable-Inhibit input. The truth table below shows the binary word required to select any one of the 16 switch positions, provided a positive logic "1" is present at the Enable Input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize voltages between 0 and 0.8 V as logic "0" voltages, and voltages between 2.4 and 15 V as logic "1" voltages. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make.

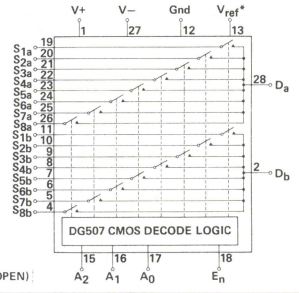
FUNCTIONAL DIAGRAMS

16 Channel MUX DG506



*OPTIONAL (NORMALLY LEFT OPEN)

8 Channel MUX DG507



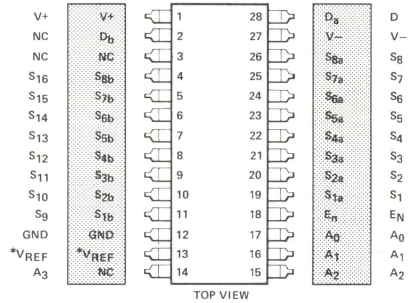
*OPTIONAL (NORMALLY LEFT OPEN)

TRUTH TABLE

A_3	A_2	A_1	A_0	E_n	ON SWITCH	
X	X	X	X	0	NONE	DG506
0	0	0	0	1	1	DG507
0	0	0	1	1	2	DG507
0	0	1	0	1	3	DG507
0	0	1	1	1	4	DG507
0	1	0	0	1	5	DG507
0	1	0	1	1	6	DG507
0	1	1	0	1	7	DG507
0	1	1	1	1	8	DG507
1	0	0	0	1	9	DG506
1	0	0	1	1	10	DG506
1	0	1	0	1	11	DG506
1	0	1	1	1	12	DG506
1	1	0	0	1	13	DG506
1	1	0	1	1	14	DG506
1	1	1	0	1	15	DG506
1	1	1	1	1	16	DG506

Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4$ V, Screen is DG507

PIN CONFIGURATIONS


DG506
DG507
Dual-In-Line Package
DG507
DG506
V+ V+ 1 28 Ds D
NC Db 2 27 V− V−
NC NC 3 26 S8a S8
S16 S8b 4 25 S7a S7
S15 S7b 5 24 S6a S6
S14 S6b 6 23 S5a S5
S13 S6b 7 22 S4a S4
S12 S4b 8 21 S3a S3
S11 S3b 9 20 S2a S2
S10 S2b 10 19 S1a S1
S9 S1b 11 18 En EN
GND GND 12 17 A0 A0
*VREF *VREF 13 16 A1 A1
A3 NC 14 15 A2 A2

TOP VIEW

*OPTIONAL (NORMALLY LEFT OPEN)

V+ COMMON TO SUBSTRATE

ORDER NUMBERS:

DG506AR OR DG506BR	DG506CJ
DG507AR OR DG507BR	DG507C
SEE PACKAGE 13	SEE PACKAGE 14

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ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, En, or V_{REF}) to Ground ..... −0.3 V, V+
V_S or V_D to V+ ..... 0, −32 V
V_S or V_D to V− ..... 0, 32 V
V+ to Ground ..... 16 V
V− to Ground ..... −16 V
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) .... 40 mA
Storage Temperature (A & B Suffix) ..... −65 to 150°C
(C Suffix) ..... −65 to 125°C
Operating Temperature (A Suffix) ..... −55 to 125°C
(B Suffix) ..... −20 to 85°C
(C Suffix) ..... 0 to 70°C
Power Dissipation (Package)*
28 Pin DIP** ..... 1200 mW
28 Pin Plastic DIP*** ..... 625 mW

*All leads soldered or welded to PC board.
**Derate 16 mW/°C above 75°C.
***Derate 8.3 mW/°C above 25°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MEASURED TERMINAL	NO. TESTS PER TEMP	(Note 1) TYP 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX −20/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Ground = 0, V_{REF} = Open (Note 4)	
1		V_{ANALOG} Minimum Analog Signal Handling Capability				±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2		$r_{DS(on)}$ Drain Source ON Resistance		S to D	16	270	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = −200 μA	Sequence each switch on
3					16	230	400	400	500	450	450	550		V_D = −10 V, I_S = −200 μA	V_{AL} = 0.8 V, V_{AH} = 2.4 V
4		$\Delta r_{DS(on)}$ Greatest Change in Drain-Source ON Resistance Between Channels		S to D	16	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)\ MAX} - r_{DS(on)\ MIN}}{r_{DS(on)\ AVE}}\right)$ −10 V ≤ V_S ≤ 10 V	
5	SWITCH	$I_{S(off)}$ Source OFF Leakage Current		S	16	−0.005		±1	±50		±5	±50	nA	V_S = 10 V, V_D = −10 V	V_{EN} = 0
6					16	−0.005		±1	±50		±5	±50		V_S = −10 V, V_D = 10 V	
7		$I_{D(off)}$ Drain OFF Leakage Current	DG506	D	1	−0.03		±10	±300		±20	±300		V_D = 10 V, V_S = −10 V	
8					1	−0.03		±10	±300		±20	±300		V_D = −10 V, V_S = 10 V	
9			DG507		2	−0.015		±5	±200		±10	±200		V_D = 10 V, V_S = −10 V	
10					2	−0.015		±5	±200		±10	±200		V_D = −10 V, V_S = 10 V	
11		$I_{D(on)}$ (Note 2) Channel ON Leakage Current	DG506	D	16	−0.06		±10	±300		±20	±300		$V_{S(all)}$ = V_D = 10 V	
12					16	−0.06		±10	±300		±20	±300		$V_{S(all)}$ = V_D = −10 V	Sequence each switch on
13			DG507		16	−0.03		±5	±200		±10	±200		$V_{S(all)}$ = V_D = 10 V	V_{AL} = 0.8 V, V_{AH} = 2.4 V
14					16	−0.03		±5	±200		±10	±200		$V_{S(all)}$ = V_D = −10 V	
15	INPUT	I_{AH} Address Input Current, Input Voltage High		A_0, A_1, A_2, (A_3) EN	(5) 4	−0.002		−10	−30		−10	−30	μA	V_A = 2.4 V	
16					(5) 4	0.006		10	30		10	30		V_A = 15 V	
17		$I_{A(peak)}$ Peak Address Input Current			(5) 4	−75								See Curve "I_A vs V_A"	
18		I_{AL} Address Input Current, Input Voltage Low			3	−0.002		−10	−30		−10	−30		V_{EN} = 2.4 V	All V_A = 0
19					1	−0.002		−10	−30		−10	−30		V_{EN} = 0	
20	DYNAMIC	$t_{transition}$ Switching Time of Multiplexer		D		0.6		1					μs	See Figure 1	
21		t_{open} Break-Before-Make Interval		D		0.2									
22		$t_{on(EN)}$ Enable Turn-ON Time		D	1	1.0		1.5						See Figure 2	
23		$t_{off(EN)}$ Enable Turn-OFF Time		D	1	0.4		1							
24		OFF Isolation (Note 3)		D		68							dB	V_{EN} = 0, R_L = 1K Ω, C_L = 15 pF V_S = 7 VRMS, f = 500 KHz	
25		$C_{S(off)}$ Source OFF Capacitance		S	16	6							pF	V_S = 0	V_{EN} = 0, f = 140 KHz
26		$C_{D(off)}$ Drain OFF Capacitance	DG506	D	1	45								V_D = 0	
27			DG507		2	23									
28	SUPPLY	I+ Positive Supply Current		V+	1	5.2		10				10	mA	V_{EN} = 5 V	All V_A = 0
29		I− Negative Supply Current		V−	1	−5.2		−10				−10			
30		I+ Positive Supply Current		V+	1	1.2		2.5				2.5		V_{EN} = 0	
31		I− Negative Supply Current		V−	1	−1.2		−2.5				−2.5			

NOTES:
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. OFF Isolation $\triangleq$ $20 \log \frac{|V_D|}{|V_S|}$ V_S = input to "OFF" switch V_D = output due to V_S.
4. Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift. For V+ = |V−| ≤ 10 V, 1.5 V may be applied to the V_{REF} terminal. The V_{REF} terminal has R_{IN} ≅ 45K Ω (See the applications section.)

DG506 ICXBA
DG507 ICXBB

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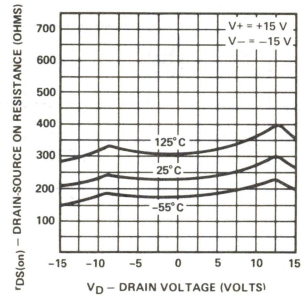
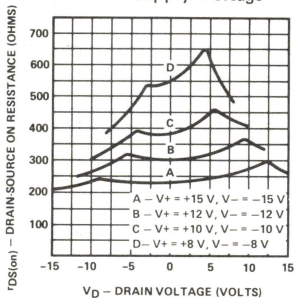
TYPICAL CHARACTERISTICS

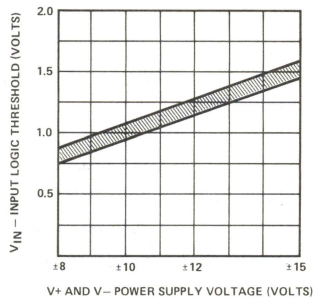
$r_{DS(on)}$ vs V_D and Temperature



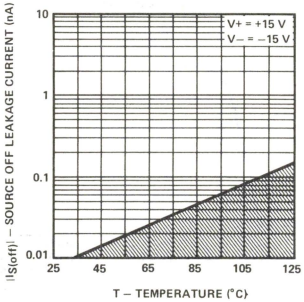
$r_{DS(on)}$ vs V_D and Power Supply Voltage



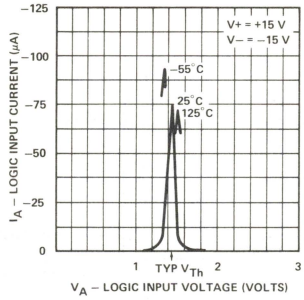
Logic Threshold vs Power Supply Voltage



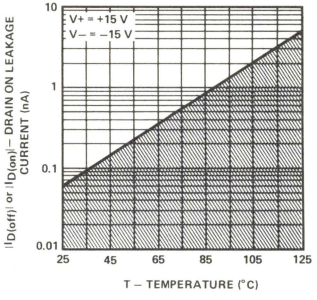
$I_{S(off)}$ vs Temperature*



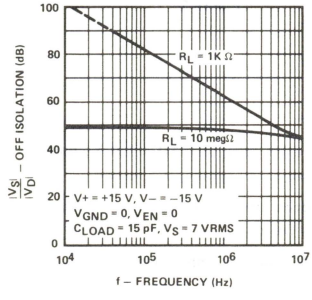
I_A vs V_A (Terminals A_0, A_1, A_2, A_3, EN)



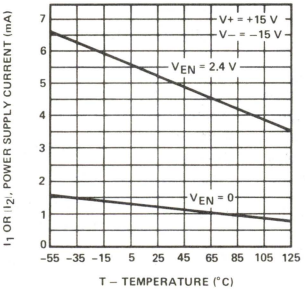
$I_{D(off)}$ and $I_{D(on)}$ vs Temperature*



OFF Isolation vs Frequency

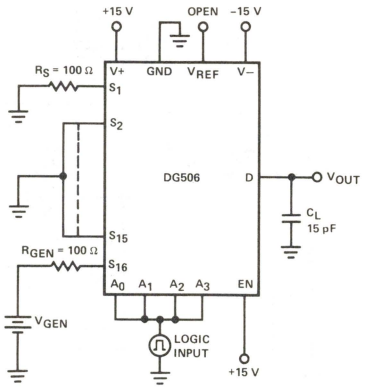


Power Supply Current vs Temperature

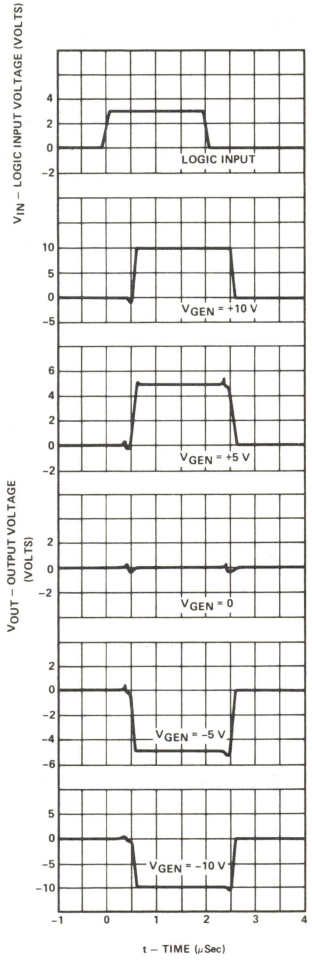


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical delay, rise, fall, settling times, and switching transients in this circuits.



If R_{GEN}, R_S, or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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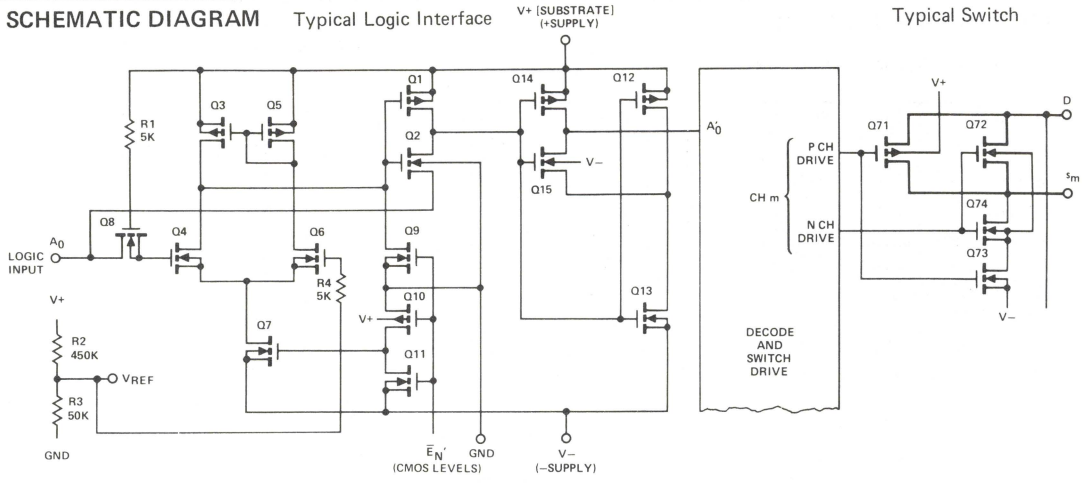
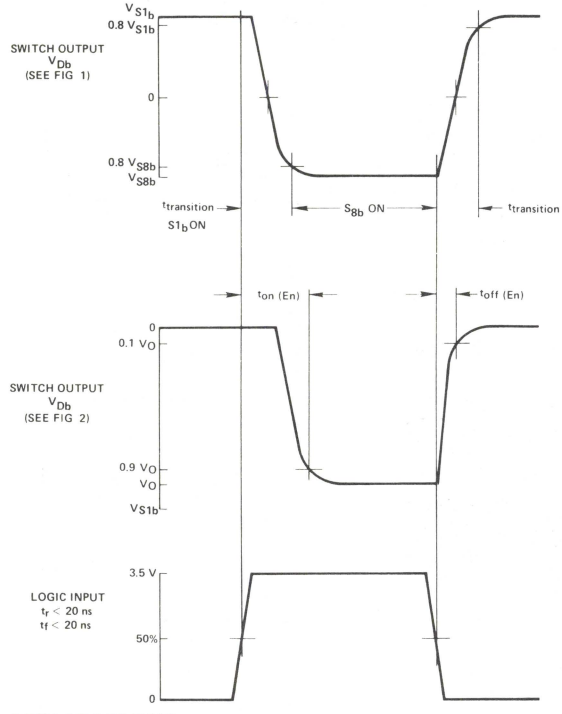
SCHEMATIC DIAGRAM

Typical Logic Interface



SWITCHING TIME TEST CIRCUIT



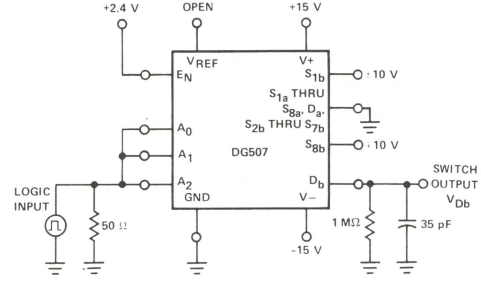


Figure 1

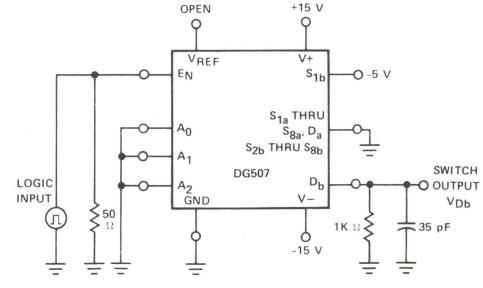


Figure 2

APPLICATIONS

Application Hints*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	−15	Open	2.4/0.8	−15 to +15
+12	−12	Open or 1.4 V	2.4/0.8	−12 to +12
+10	−10	1.4 V	2.4/0.8	−10 to +10
+8***	−8	1.4 V	2.4/0.8	−8 to +8

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V− = −15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended.

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8-Channel/4-Channel Differential CMOS Analog Multiplexer *designed for...*

- **Data Acquisition Systems**
- **Multiplexing Reference Signals**
- **Communication Systems**

BENEFITS

- **Easily Interfaced**
  - TTL, DTL and CMOS Direct Control Over Military Temperature Range
- **Low Stand-By Power**
  - 36 mW Typical Stand-By Power
- **Reduces System Cross-Talk**
  - Break-Before-Make Switching Action
- **Reduces External Component Requirements**
  - ±15 V Analog Signal Range with ±15 V Supplies
- **Environmentally Rugged**
  - Latch-proof CMOS

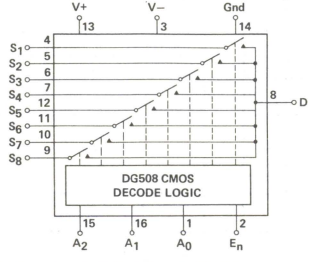
DESCRIPTION

The DG508 is a single-pole 8-position (plus OFF) electronic switch array [DG509 double-pole, 4-position (plus OFF)], which employs 8 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction, and in the OFF position each switch will block voltages up to 30 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word input plus an Enable-Inhibit input. The truth table below shows the binary word required to select any one of the 8 switch positions, provided a positive logic "1" is present at the Enable Input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize as logic "0" any voltage between 0 and 0.8 V, and any voltage between 2.4 and 15 V as logic "1" inputs. The inputs can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Delays are designed into logic decode and driver circuits to insure that switch action is break-before-make.

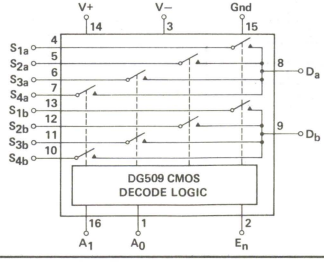
DECODE TRUTH TABLE

	A_2	A_1	A_0	En	ON SWITCH	DG509
DG508	X	X	X	0	NONE	
	0	0	0	1	1	
	0	0	1	1	2	
	0	1	0	1	3	
	0	1	1	1	4	
	1	0	0	1	5	Logic "1" = $V_{AH} \geq 2.4$ V
	1	0	1	1	6	
	1	1	0	1	7	Logic "0" = $V_{AL} \leq 0.8$ V
	1	1	1	1	8	

FUNCTIONAL DIAGRAM DG508

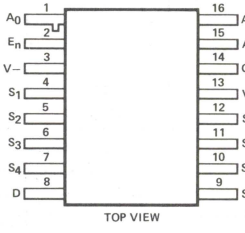


FUNCTIONAL DIAGRAM DG509



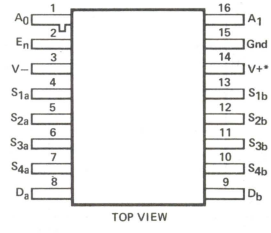
PIN CONFIGURATIONS

Flat Package



ORDER NUMBER:
DG508AL
SEE PACKAGE 17

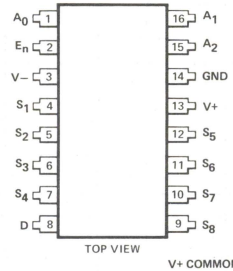
Flat Package



ORDER NUMBER:
DG509AL
SEE PACKAGE 17

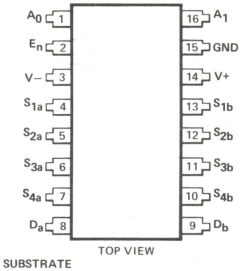
*Common to Substrate and Base of Package

Dual-In-Line Package



ORDER NUMBERS:
DG508AP OR DG508BP
SEE PACKAGE 12
DG508CJ
SEE PACKAGE 8

Dual-In-Line Package



V+ COMMON TO SUBSTRATE

ORDER NUMBERS:
DG509AP OR DG509BP
SEE PACKAGE 12
DG509CJ
SEE PACKAGE 8

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ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground . . . . . −0.3 V, V+
V_S or V_D to V+ . . . . . 0, −32 V
V_S or V_D to V− . . . . . 0, 32 V
V+ to Ground . . . . . 16 V
V− to Ground . . . . . −16 V
Current (Any Terminal, Except S or D) . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) . . 40 mA
Operating Temperature (A Suffix) . . . . −55 to 125°C
(B Suffix) . . . . −20 to 85°C
(C Suffix) . . . . 0 to 70°C
Storage Temperature (A & B Suffix) . . −65 to 150°C
(C Suffix) . . . . −65 to 125°C
Power Dissipation (Package)*
16 Pin DIP** . . . . . 900 mW
16 Pin Plastic DIP*** . . . . . 470 mW
Flat Package**** . . . . . 750 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.3 mW/°C above 25°C
****Derate 10 mW/°C above 75°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MEASURED TERMINAL	NO. TESTS PER TEMP.	TYP† 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIXES −20°C 0°C	B/C SUFFIXES 25°C	B/C SUFFIXES 85°C 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = 15 V, Ground = 0
1		V_{ANALOG}	Minimum Analog Signal Handling Capability Capability			±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA
2		$r_{DS(on)}$	Drain-Source ON Resistance	S to D	8	270	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = −200 μA; Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
3					8	230	400	400	500	450	450	500		V_D = −10 V, I_S = −200 μA
4		$\Delta r_{DS(on)}$	Greatest Change in Drain Source ON Resistance Between Channels	S to D	8	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ MAX - r_{DS(on)}\ MIN}{r_{DS(on)}\ AVE}\right)$ −10 V ≤ V_S ≤ 10 V
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	S	8	−0.005		±1	±50		±5	±50	nA	V_S = 10 V, V_D = −10 V; V_{EN} = 0
6					8	−0.005		±1	±50		±5	±50		V_S = −10 V, V_D = 10 V
7		$I_{D(off)}$	Drain OFF Leakage Current DG508	D	1	−0.015		±10	±200		±20	±200		V_D = 10 V, V_S = −10 V
8					1	−0.015		±10	±200		±20	±200		V_D = −10 V, V_S = 10 V
9			DG509		2	−0.008		±10	±100		±20	±100		V_D = 10 V, V_S = −10 V
10					2	−0.008		±10	±100		±20	±100		V_D = −10 V, V_S = 10 V
11		$I_{D(on)}$*	Drain ON Leakage Current DG508	D	8	−0.03		±10	±200		±20	±200		$V_{S(all)}$ = V_D = 10 V; Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
12					8	−0.03		±10	±200		±20	±200		$V_{S(all)}$ = V_D = −10 V
13			DG509		8	−0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = 10 V
14					8	−0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = 10 V
15	INPUT	I_{AH}	Address Input Current, Input Voltage High	A_0, A_1 (A_2) EN	(4) 3	−0.002		−10	−30		−10	−30	μA	V_A = 2.4 V
16					(4) 3	0.006		10	30		10	30		V_A = 15 V
17		$I_{A(peak)}$	Peak Address Input Current		(4) 3	−75								See Curve "I_A vs V_A"
18		I_{AL}	Address Input Current Input Voltage Low	A_0, A_1 (A_2)	3	−0.002		−10	−30		−10	−30		V_{EN} = 2.4 V; All V_A = 0
19				EN	1	−0.002		−10	−30		−10	−30		V_{EN} = 0
20	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer	D		0.6		1					μs	See Figure 1
21		t_{open}	Break-Before-Make Interval	D		0.2								
22		$t_{on(EN)}$	Enable Turn-ON Time	D	1	1.0		1.5						See Figure 2
23		$t_{off(EN)}$	Enable Turn-OFF Time	D	1	0.4		1						
24		OFF Isolation**		D	8	68							dB	V_{EN} = 0, R_L = 1K Ω, C_L = 15 pF V_S = 7 VRMS, f = 500 kHz
25		$C_{S(off)}$	Source OFF Capacitance	S	8	5							pF	V_S = 0; V_{EN} = 0, f = 140 kHz
26		$C_{D(off)}$	Drain OFF Capacitance DG508	D	1	25								V_D = 0
27			DG509	D	2	12								
28	SUPPLY	I+	Positive Supply Current	V+	1	3.5		8.0			8.0		mA	V_{EN} = 5 V; All V_A = 0
29		I−	Negative Supply Current	V−	1	−3.5		−8.0			−8.0			
30		I+ Standby	Positive Supply Current	V+	1	1.0		2.4			2.8			V_{EN} = 0
31		I− Standby	Negative Supply Current	V−	1	−1.0		−2.4			−2.8			

ICXG-A DG508
ICGX-B DG509

† Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

*$I_{D(on)}$ is leakage from driver into "ON" switch.

**OFF isolation $\triangleq 20 \log \frac{|V_D|}{|V_S|}$, V_S = input to "OFF" switch, V_D = output due to V_S.

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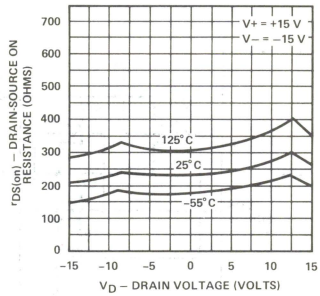
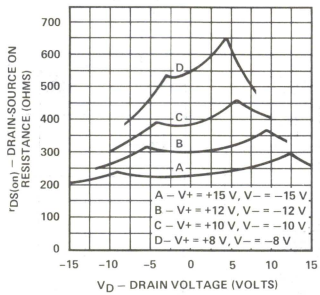
TYPICAL CHARACTERISTICS

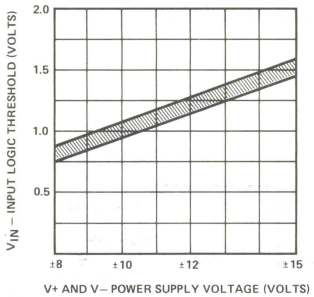
$r_{DS(on)}$ vs V_D and Temperature



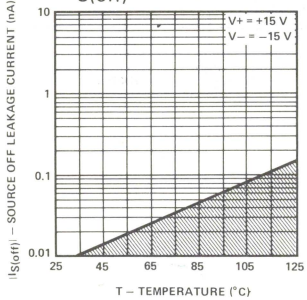
$r_{DS(on)}$ vs V_D and Power Supply Voltage



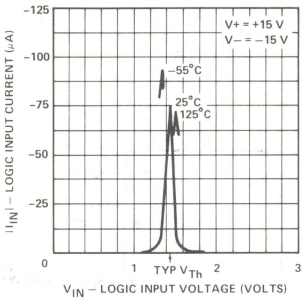
Logic Threshold vs Power Supply Voltage



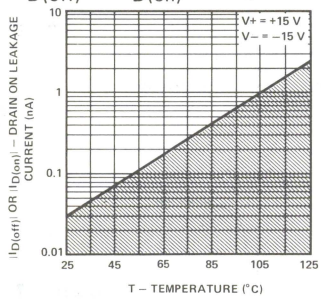
$I_{S(off)}$ vs Temperature*



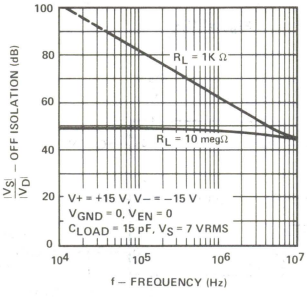
I_A vs V_A (Terminals A_0, A_1, A_2, EN)



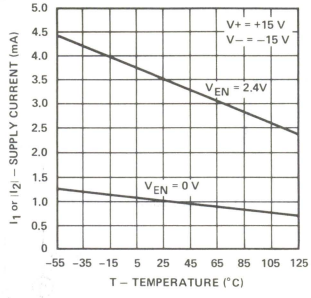
$I_{D(off)}$ and $I_{D(on)}$ vs Temperature*



OFF Isolation vs Frequency

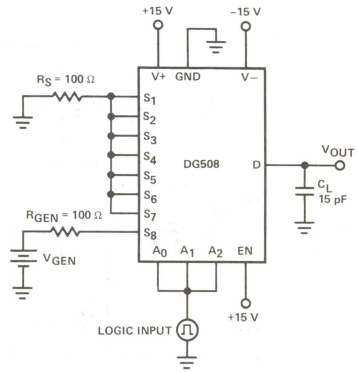


Power Supply Current vs Temperature

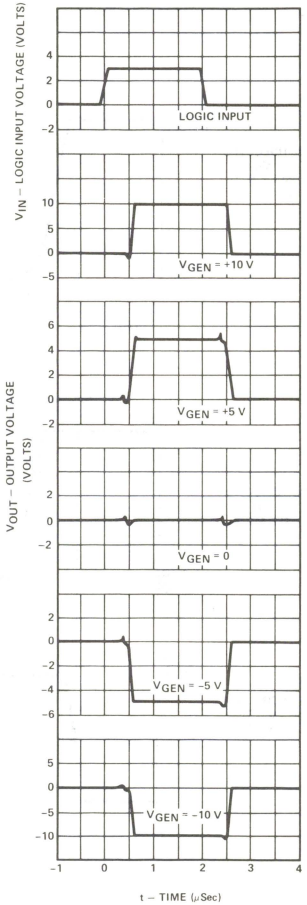


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical delay, rise, fall, settling times, and switching transients in this circuit (similar circuit for DG509).



If R_{GEN}, R_S, or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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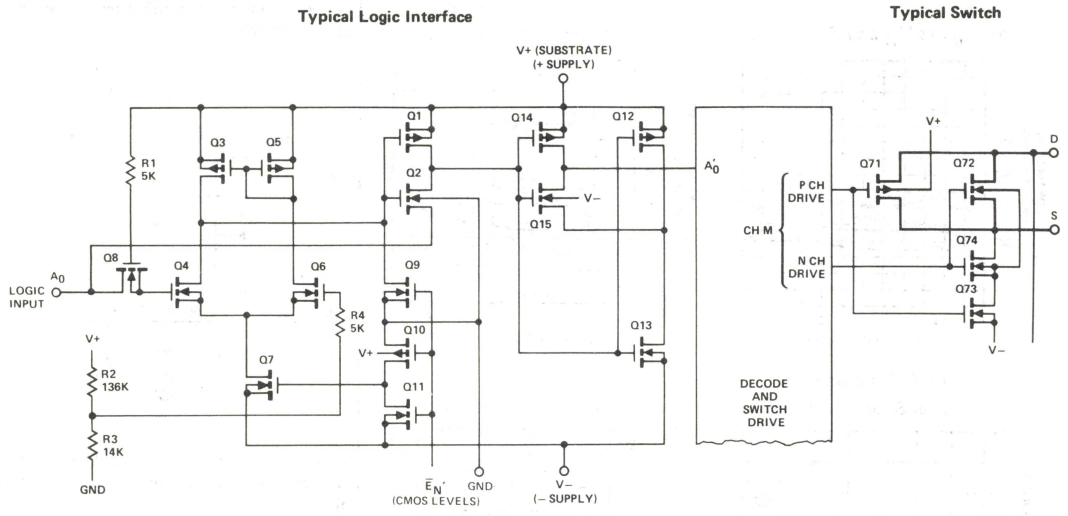
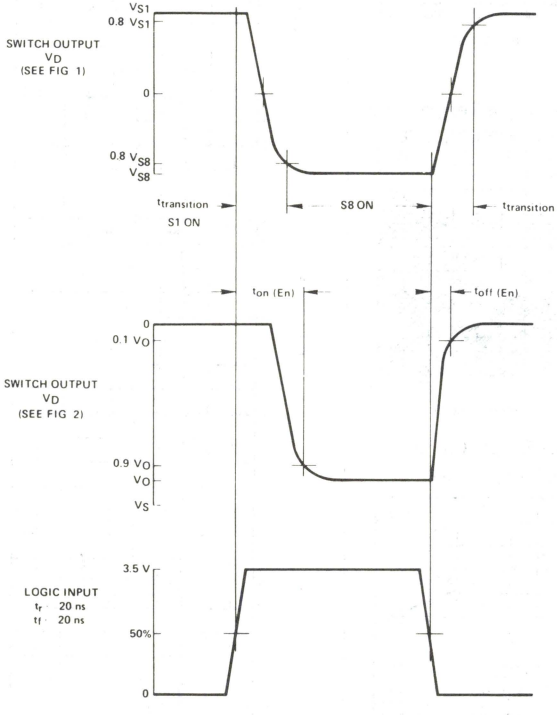
SCHEMATIC DIAGRAM



SWITCHING TIME TEST CIRCUIT



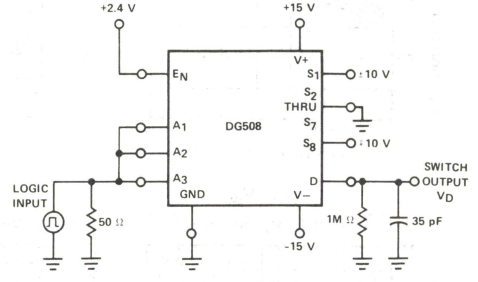


Figure 1(a)

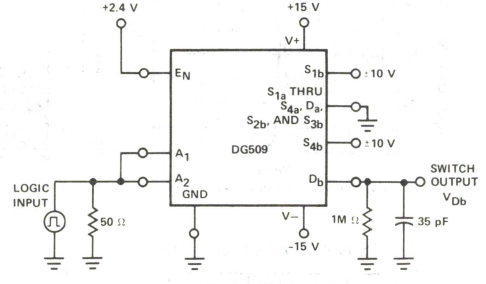


Figure 1(b)

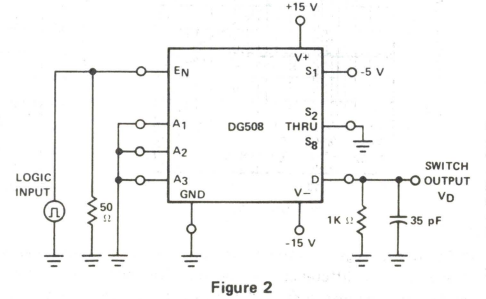


Figure 2

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APPLICATIONS

Application Hints*

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	−15	Open	2.4/0.8	−15 to +15
+12	−12	Open or 1.4 V	2.4/0.8	−12 to +12
+10	−10	1.4 V	2.4/0.8	−10 to +10
+8***	−8	1.4 V	2.4/0.8	−8 to +8

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V− = −15 V.

***Operation below ±8 V is not recommended due to the shift in V_{REF}.

Logic Inputs

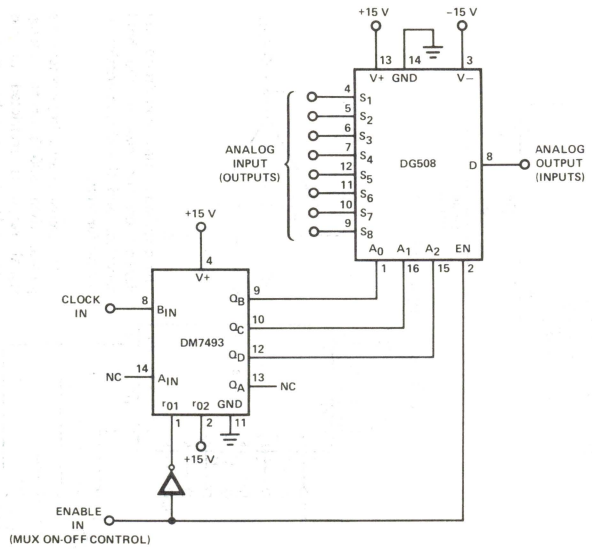
Logic input circuitry protects the input MOS gate from static transients. A series MOS device shuts off when V_{IN} exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from V_{INH} to V_{INL}. If a series resistor is used for additional static protection, it should be limited to less than 9.1K Ω to insure switching with worst case current spikes.

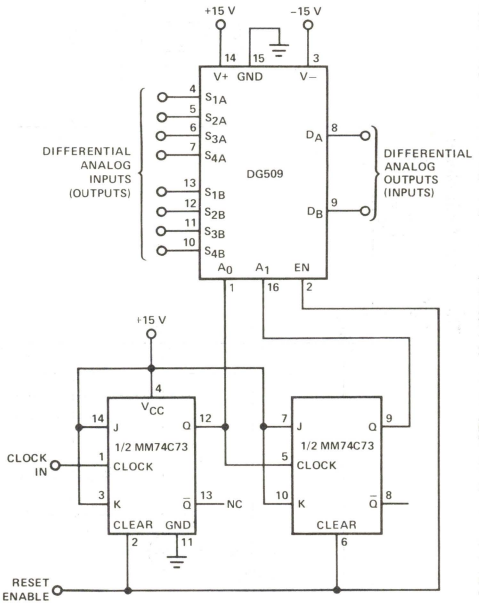
Truth Table

	ENABLE	MUX SEQUENCE RATE	MUX INPUTS A_0	A_1	A_2	DG508 SWITCH PAIR STATES (– DENOTES OFF) S1	S2	S3	S4	S5	S6	S7	S8
DG509	0	0	X	X	X	–	–	–	–	–	–	–	–
	1	0	0	0	0	ON	–	–	–	–	–	–	–
	1	1 pulse	1	0	0	–	ON	–	–	–	–	–	–
	1	2 pulses	0	1	0	–	–	ON	–	–	–	–	–
	1	3 pulses	1	1	0	–	–	–	ON	–	–	–	–
	1	4 pulses	0	0	1	–	–	–	–	ON	–	–	–
	1	5 pulses	1	0	1	–	–	–	–	–	ON	–	–
	1	6 pulses	0	1	1	–	–	–	–	–	–	ON	–
	1	7 pulses	1	1	1	–	–	–	–	–	–	–	ON
	1	8 pulses	0	0	0	ON	–	–	–	–	–	–	–

8 Channel Sequential Mux (Demux)



Differential 4 Channel Sequential Mux/Demux.



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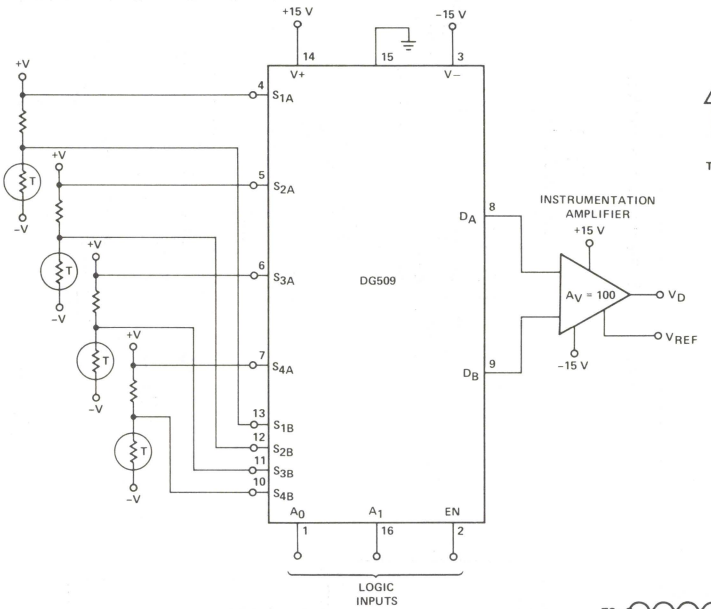
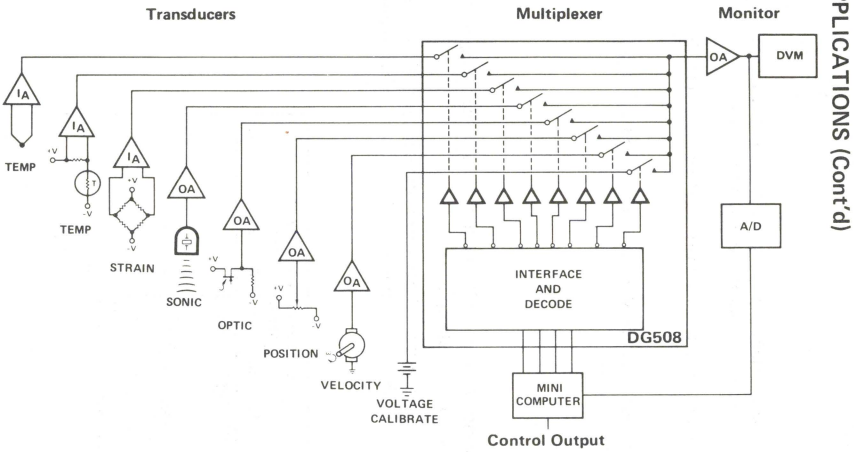
APPLICATIONS (Cont'd)

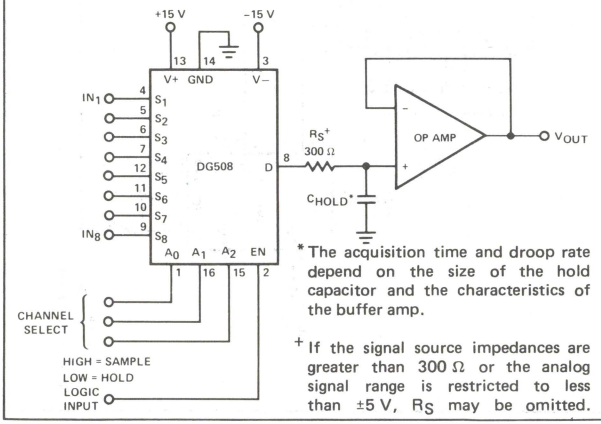
Thermistor Multiplexer



Industrial Control Multiplexing



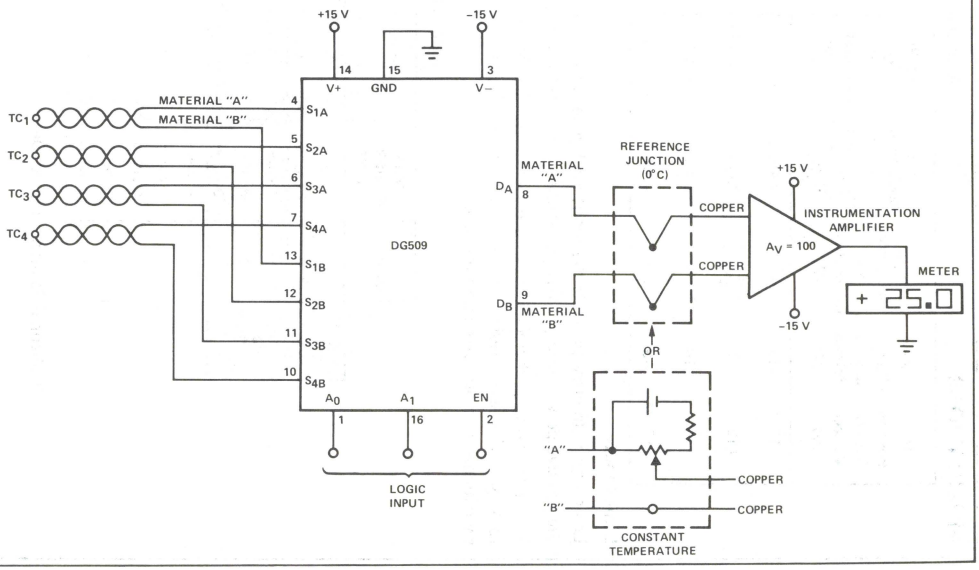
8 Input Sample-and-Hold



* The acquisition time and droop rate depend on the size of the hold capacitor and the characteristics of the buffer amp.

\+ If the signal source impedances are greater than 300 Ω or the analog signal range is restricted to less than ±5 V, R_S may be omitted.

DG509 Thermocouple Multiplexer



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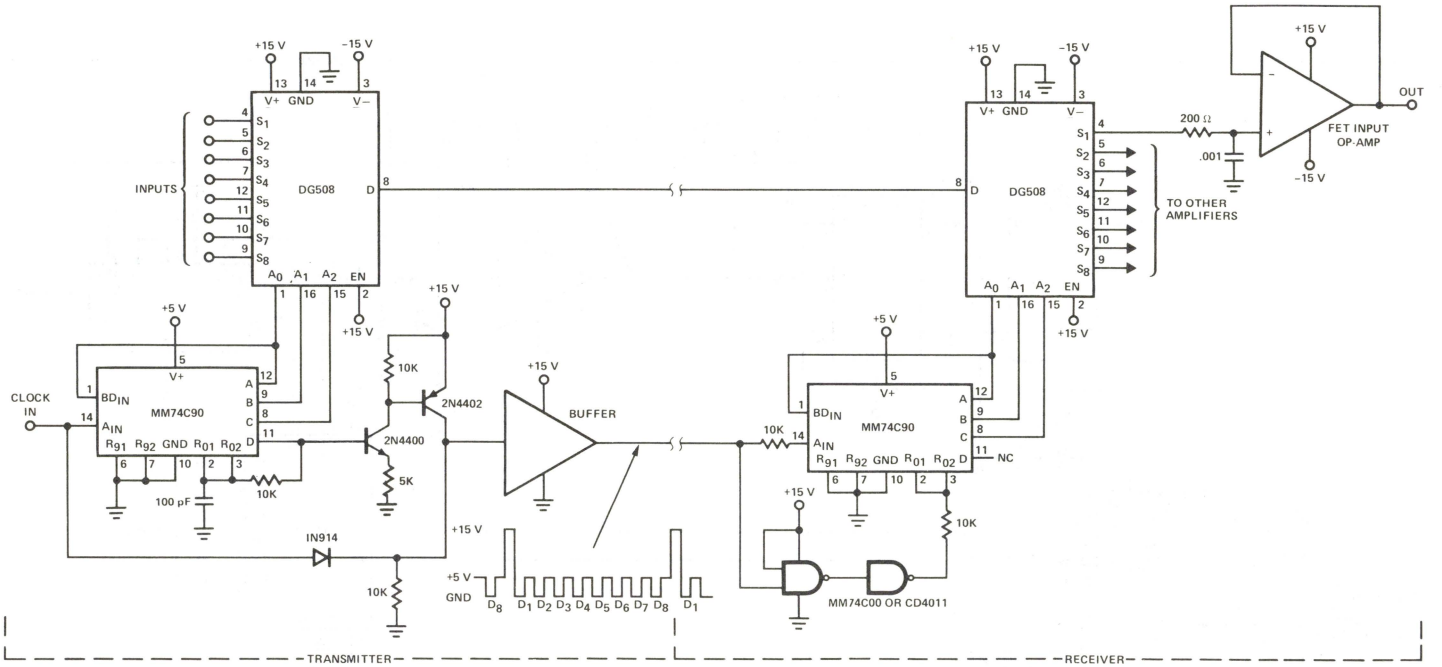
An 8 Channel Mux/Demux System



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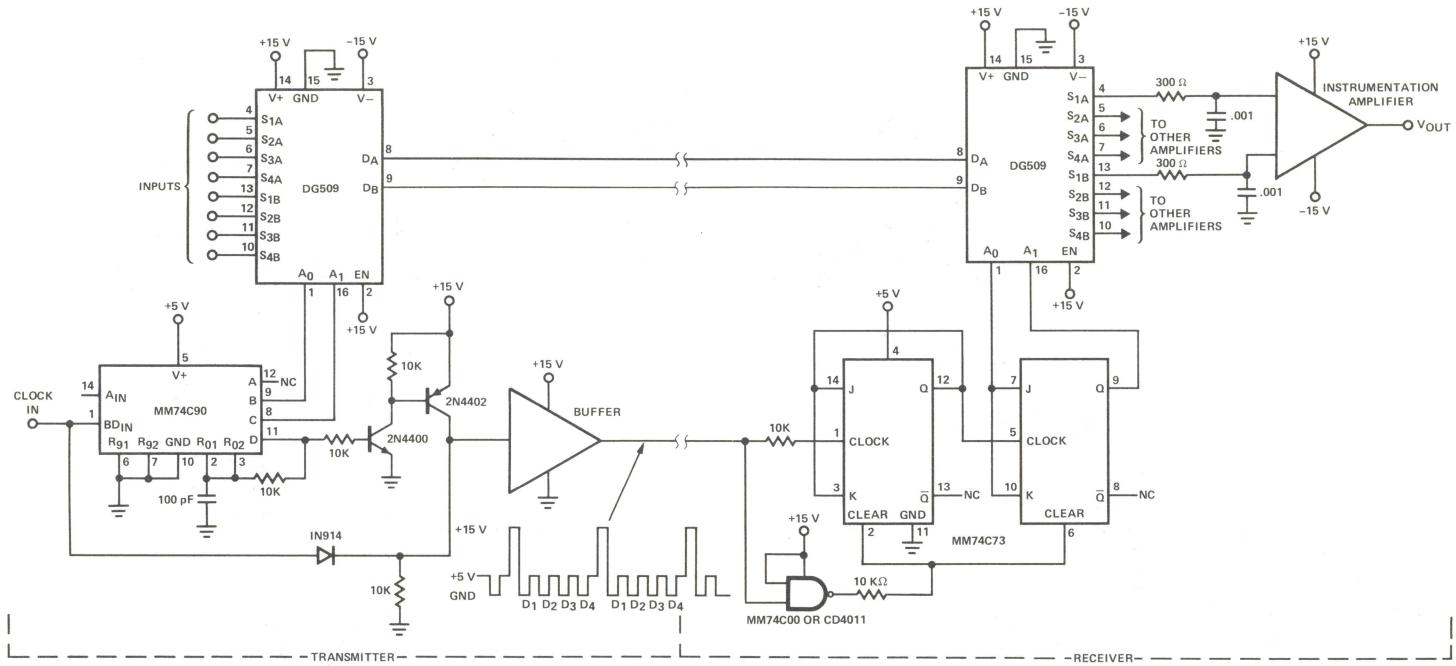
Differential Mux/Demux System



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D/A Converter Switches

designed for . . .

- **4, 10 or 14 Bit DACs**
- **Binary or BCD DACs**
- **Multiplying DACs**
- **Successive Approximation ADC**
- **Frequency Synthesizers**
- **Virtual Ground Switches**

BENEFITS

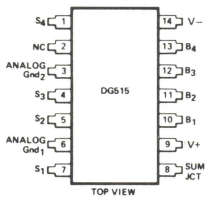
- **Easily Interfaced**
  - Binary Weighting of ON Resistances
- **Minimizes System Power Requirements**
  - 40 μW Operating Power
- **Reduces Systems Costs**
  - Single Supply Operation

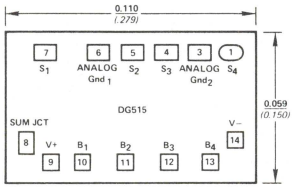
DESCRIPTION

The DG515 and DG516, 4 and 10 bit SPDT switches, combine NMOS analog switches with CMOS switch drivers. These switches feature low channel ON resistance, binary weighting of ON resistance and channel resistance matching to minimize the errors that can lead to non-monotonicity in D/A converters. The binary ON resistance weighting (doubling for each bit) is continued from the DG515 to the DG516 to allow the pair to be used as a 14 bit DAC.

PIN CONFIGURATIONS/BONDING DIAGRAMS

Dual In-Line Package

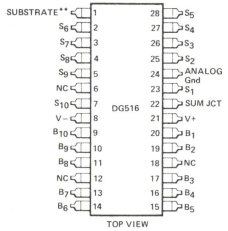


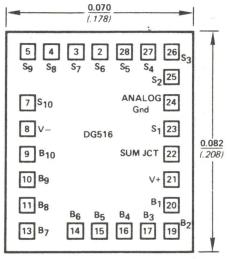


ORDER NUMBERS:
DG515AP
DG515BP
SEE PACKAGE 11
DG515CJ
SEE PACKAGE 7

*** ORDER NUMBERS:**
DG515ADICE
DG515BDICE
DG515CDICE

Dual In-Line Package





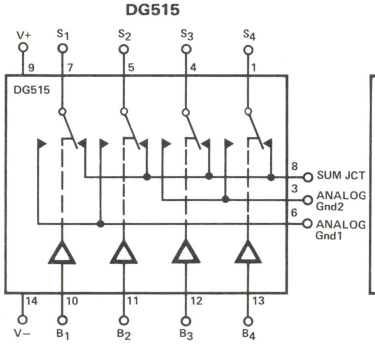
ORDER NUMBERS:
DG516AR
DG516BR
SEE PACKAGE 13
DG516CJ
SEE PACKAGE 14

*** ORDER NUMBERS:**
DG516ADICE
DG516BDICE
DG516CDICE

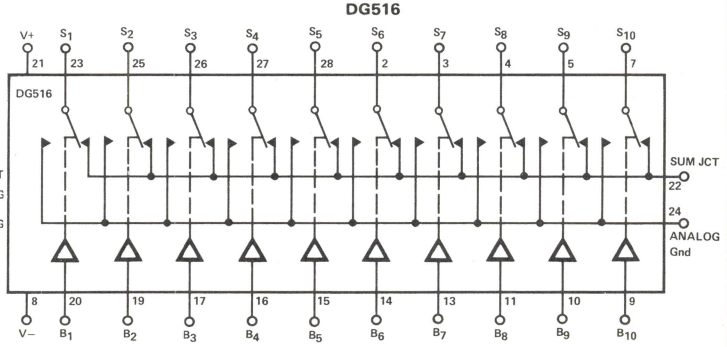
* CONTACT FACTORY FOR TESTING AND INSPECTION CRITERIA
** SHOULD BE LEFT UNCONNECTED OR CAN BE TIED TO V^+

FUNCTIONAL DIAGRAMS

DG515



DG516



SWITCH STATES ARE FOR LOGIC "1" INPUT

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ABSOLUTE MAXIMUM RATINGS

V_S to Sum Jct or Analog Gnd . . . . . −200 mV
V_{IN} (Bit Logic Input)† . . . . . $V- \leq V_{IN} \leq V+$
I_{SWITCH} . . . . . 10 mA
Current (Any Terminal Except Switch) . . . 30 mA
Storage Temperature (A & B Suffix) . . −65 to 150°C
(C Suffix) . . . . −65 to 125°C
Operating Temperature
(A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
(C Suffix) . . . . . 0 to 70°C
Power Dissipation (Package)*
14 Pin Ceramic DIP** . . . . . 825 mW
14 Pin Plastic DIP*** . . . . . 470 mW
28 Pin Ceramic DIP**** . . . . . 1200 mW
28 Pin Plastic DIP***** . . . . . 625 mW

*Device mounted with all leads welded or soldered to PC board
**Derate 11 mW/°C above 70°C
***Derate 6.3 mW/°C above 25°C
****Derate 10 mW/°C above 25°C
*****Derate 8.3 mW/°C above 25°C

†NOTE: Exceeding these voltage limits can result in a latch-up condition, excessive I+ and possible destruction to the device. Placing a 2K Ω resistor in series with V+ will protect the device and allow recovery (without power supply cycling) after the overvoltage is removed.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters to assure conformance with specifications. DICE are sorted by DC parameter tests and visual inspections.

		Characteristic		DG515	DG515 MAX LIMITS						DG516	DG516 MAX LIMITS						Unit	Test Conditions $V+ = 8.0$ V, $V- = 0$ V
					DG515A/B			DG515C				DG516A/B			DG516C				
				Typ† @ 25°C	−55°C To −20°C	25°C	125°C To 85°C	0°C	25°C	70°C	Typ† @ 25°C	−55°C To −20°C	25°C	125°C To 85°C	0°C	25°C	70°C		
1	SWITCH	$r_{DS(on)}$	Switch 1		6.25	6.25	9.0	7.8	7.8	11.2								Ω	$I_S = 10$ mA
2	SWITCH	$r_{DS(on)}$	Switch 2		12.5	12.5	18.0	15.6	15.6	22.5									
3	SWITCH	$r_{DS(on)}$	Switch 3		25.0	25.0	36.0	31.2	31.2	45.0									
4	SWITCH	$r_{DS(on)}$	Switch 4		50.0	50.0	72.0	62.5	62.5	90.0									
5	SWITCH	$r_{DS(on)}$	Switch 1									100	100	144	125	125	180		$I_S = 1.0$ mA
6	SWITCH	$r_{DS(on)}$	Switch 2									200	200	288	250	250	360		
7	SWITCH	$r_{DS(on)}$	Switch 3									400	400	576	500	500	720		
8	SWITCH	$r_{DS(on)}$	Switch 4									800	800	1150	1000	1000	1440		
9	SWITCH	$r_{DS(on)}$	Switch 5									1600	1600	2300	2000	2000	2880		$I_S = 0.1$ mA
10	SWITCH	$r_{DS(on)}$	Switch 6–10									3200	3200	4600	4000	4000	5760		
11	SWITCH	$\Delta r_{DS(on)}$	Switch to ANLG GND Switch to SUM JCT	20**							20**							%	$V_{INH} = 8.0$ V, $V_{INL} = 0$ V
12	INPUT	$I_{D(off)}$	$I_{ANALOG\ Gnd\ (off)}$		100	40	2000	100	40	2000		100	40	2000	100	40	2000	nA	$V_{ANALOG\ Gnd} = 0$ V, $V_S = -100$ mV
13	INPUT	$I_{D(off)}$	$I_{SUMMING\ Junction\ (off)}$		100	40	2000	100	40	2000		100	40	2000	100	40	2000		$V_{SUMMING\ Jct} = 0$ V, $V_S = -100$ mV
14	INPUT	V_{IN}	Threshold	4.0							4.0							V	
15	INPUT	I_{INL}	Input Current Input Voltage Low		−1.0	−1.0	−1.0	−1.0	−1.0	−1.0		−1.0	−1.0	−1.0	−1.0	−1.0	−1.0	μA	$V_{INL} = 0$ V
16	INPUT	I_{INH}	Input Current Input Voltage High		+1.0	+1.0	+1.0	+1.0	+1.0	+1.0		+1.0	+1.0	+1.0	+1.0	+1.0	+1.0		$V_{INH} = 8.0$ V
17		t_{on}	Turn-ON Time			120			180				120			180		ns	See Switching Time Test Circuit
18		t_{off}	Turn-OFF Time			170			250				170			250			
19		C_D	Output Capacitance ANLG GND	60							20							pF	$V_{INL} = 0$ V f = 1 MHz
20		C_D	Output Capacitance SUM JCT	40							14								
21		C_D	Output Capacitance ANLG GND	40							14							pF	$V_{INH} = 8.0$ V f = 1 MHz
22		C_D	Output Capacitance SUM JCT	60							20								
23		I+	Positive Supply Current		5.0	5.0	150	5.0	5.0	150		5.0	5.0	150	5.0	5.0	150	μA	$V_{INH} = 8.0$ V
24		I−	Negative Supply Current		−5.0	−5.0	−150	−5.0	−5.0	−150		−5.0	−5.0	−150	−5.0	−5.0	−150		
25		I+	Positive Supply Current		5.0	5.0	150	5.0	5.0	150		5.0	5.0	150	5.0	5.0	150		$V_{INL} = 0$ V
26		I−	Negative Supply Current		−5.0	−5.0	−150	−5.0	−5.0	−150		−5.0	−5.0	−150	−5.0	−5.0	−150		

NOTES:
† Typical values are for Design Aid only, not guaranteed and not subject to production testing.
* Delta $r_{DS(on)}$ as percent of maximum resistance.
** This is the worst typical mismatch seen on a device.

DG515-ICAS
DG516-ICAT

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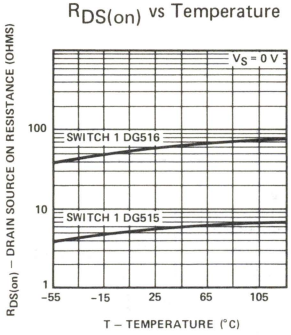
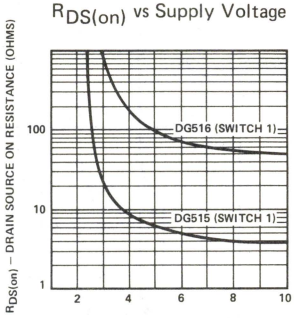
TYPICAL CHARACTERISTICS

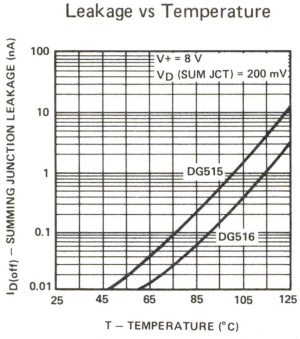
$R_{DS(on)}$ vs Temperature



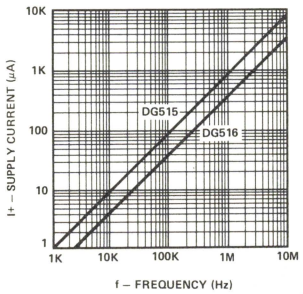
$R_{DS(on)}$ vs Supply Voltage



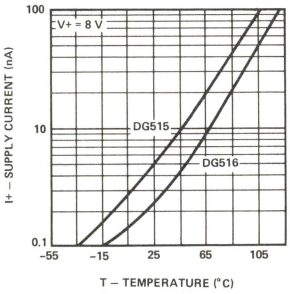
Leakage vs Temperature



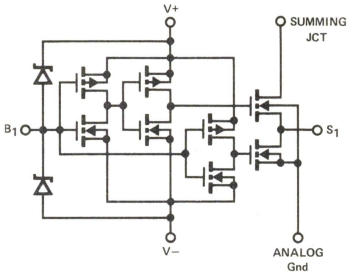
Supply Current vs Toggling Rate



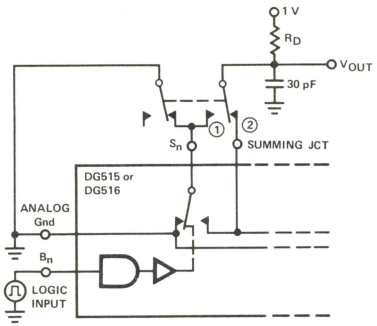
Quiescent Supply Current vs Temperature



Typical Channel (DG515 or DG516)

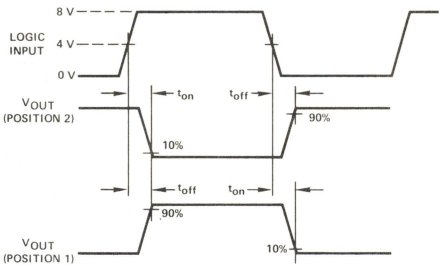


Switching Time Test Circuit



SWITCH	R_D (ohms)	
	DG515	DG516
1	50	300
2	100	300
3	200	300
4	200	510
5		510
6		1000
7		1000
8		1000
9		1000
10		1000

Switching Test Waveforms



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APPLICATIONS

The following Application Circuits are intended to illustrate the following points:

1. A 2K Ω resistor should be in series with V+ to limit supply current with negative ringing of the bit inputs.
2. Temperature compensation for $R_{DS(on)}$ can be provided in the feedback path of the Op-Amp.
3. 4 Quadrant multiplication is possible by using the Analog Gnd current.
4. Bipolar reference voltages can be used in all configurations.
5. Resistor weighting other than Binary can be used.

4 Bit Multiplying Current Switch D/A

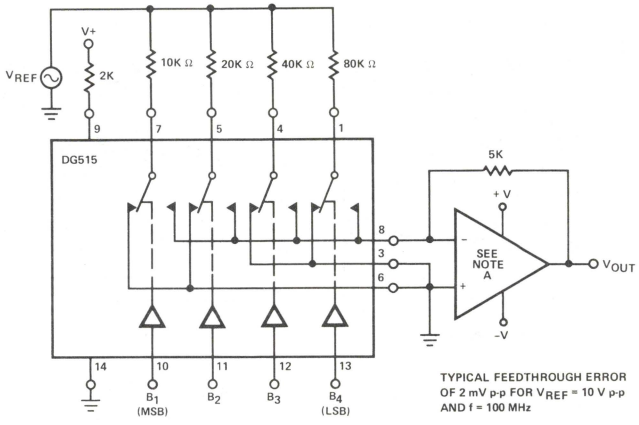

Figure 1

10 Bit D/A Converter

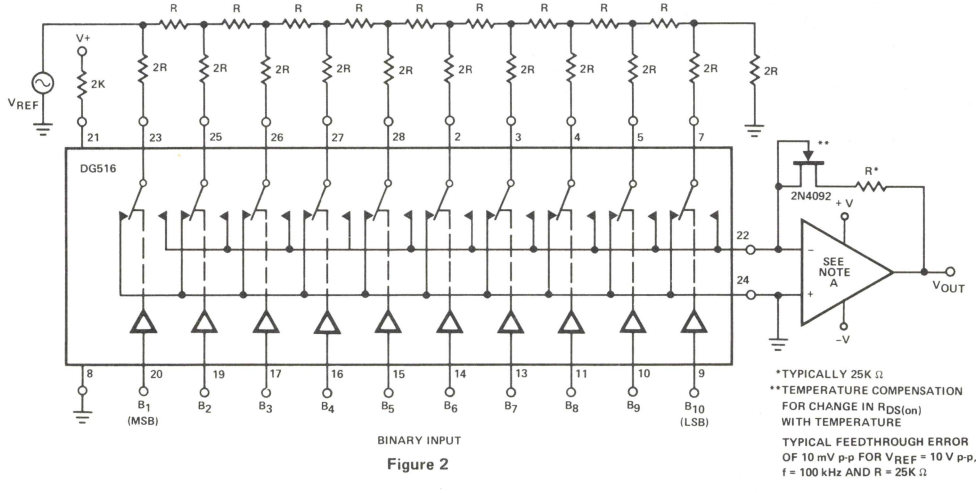

Figure 2

Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2+2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2-2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Figure 3

NOTE:

A. Op-Amp characteristics effect D/A accuracy and settling time. The following Op-Amps, listed in order of increasing speed, are suggested:

1. LM101A
2. LF156A
3. LM118

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APPLICATIONS (Cont'd)

10 Bit, 4 Quadrant Multiplying DAC
(Offset Binary Coding)

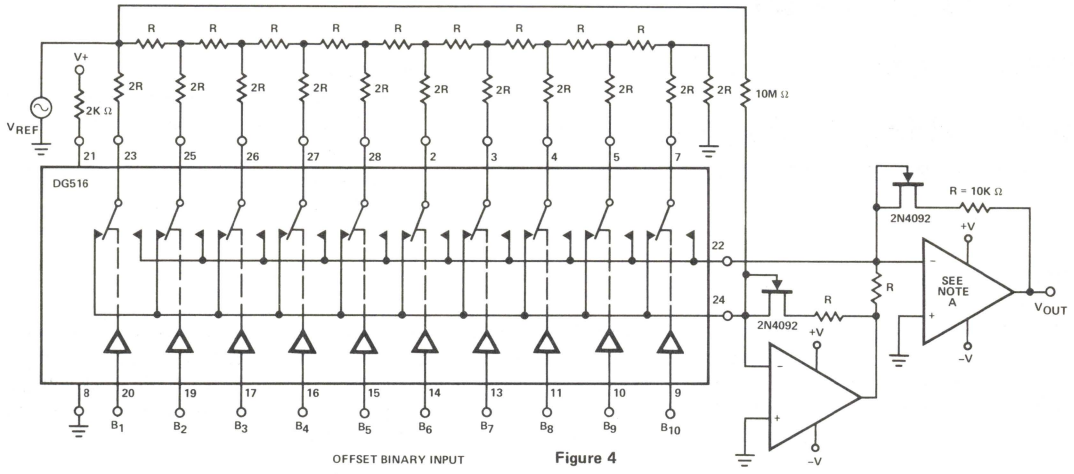

Figure 4

Bipolar (Offset Binary)* Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}
NOTE: 1 LSB = $2^{-9}\ V_{REF}$	
*Complementing B_1 (MSB) will give 2's complement coding.	

Figure 5

Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-14})$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-14})$
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Figure 6

14 Bit Binary DAC (unipolar)

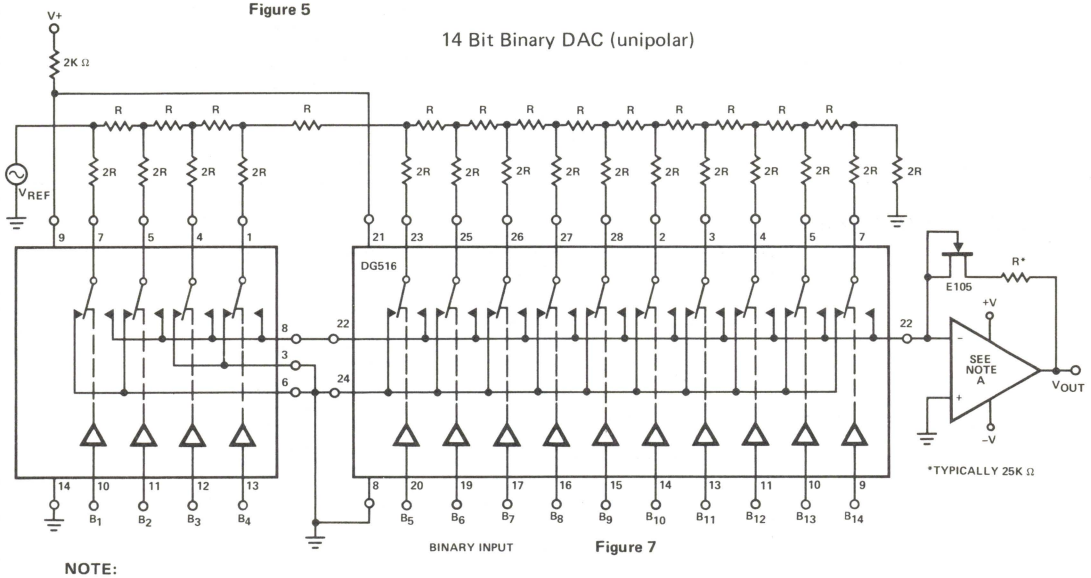

Figure 7

NOTE:

A. Op-Amp characteristics effect D/A accuracy and settling time. The following Op-Amps, listed in order of increasing speed, are suggested:

1. LM101A
2. LF156A
3. LM118

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Monolithic SPST MOS Switch with Driver

Siliconix

designed for . . .

- **Switching Analog Signals such as Reference Signals**

BENEFITS

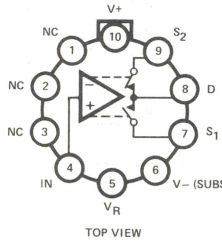
- **Reduces External Component Requirements**
  - Internal Zener Diodes Protect All MOS Gates
- **Easily Interfaced**
  - TTL and DTL Integrated Logic

DESCRIPTION

The SI3002 contains two P-channel MOS field-effect transistors designed to function as single-pole double-throw electronic switches. A level-shifting driver enables a low-level input (0.8 to 2 V) to control the ON-OFF state of the switches. In the ON state, each switch will conduct current equally well in either direction. In the OFF state the switches will block voltages up to 20 V peak-to-peak. With logic "0" at the driver input, a common drain (D) is connected through an ON switch to source (S_1). With logic "1" at the input, "D" is connected to S_2. Switch action is make-before-break.

PIN CONFIGURATIONS

Metal Can Package

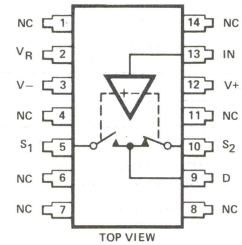


TOP VIEW

LOGIC	SW 1	SW 2
0	ON	OFF
1	OFF	ON

ORDER NUMBER: Si3002AA
SEE PACKAGE 2

Dual-In-Line Package

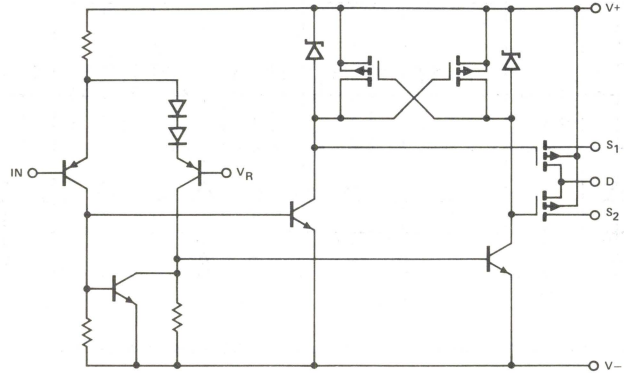


TOP VIEW

ORDER NUMBER: Si3002BP
SEE PACKAGE 11

LOGIC STATES ARE FOR LOGIC "1" INPUT
(POSITIVE LOGIC)

SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

V+ to V–	36 V
V+ to V_S or V_D	25 V
V+ to V_R or V_{IN}	12 V
V_D to V–	36 V
V_S to V–	36 V
V_D to V_S	±25 V
V_{IN} to V_R	±6 V
Current (Any Terminal)	30 mA
Storage Temperature	–65 to 150°C
Operating Temperature (A Suffix)	–55 to 125°C
(B Suffix)	–20 to 85°C

Power Dissipation*

Metal Can** 450 mW

14 Pin DIP*** 825 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 6 mW/°C above 75°C.

***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

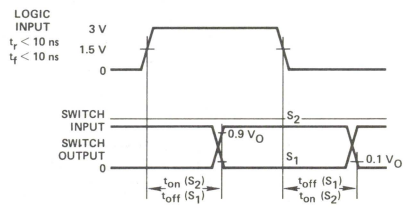
		CHARACTERISTIC		MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B SUFFIX –20°C	B SUFFIX 25°C	B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V– = –20 V, V_R = 0		
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	100	100	150	100	100	150	Ω	V_D = 10 V	I_S = –1 mA	V_{INL} = 0.8 V (Sw_1 ON) V_{INH} = 2.0 V (Sw_2 ON)
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	250	150	150	250	Ω	V_D = 0	I_S = –1 mA	V_{INL} = 0.8 V (Sw_1 ON) V_{INH} = 2.0 V (Sw_2 ON)
3	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	400	400	500	400	400	500	Ω	V_D = –10 V	I_S = –1 mA	V_{INL} = 0.8 V (Sw_1 ON) V_{INH} = 2.0 V (Sw_2 ON)
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		–1	–1000		–5	–100	nA	V_S = –10 V, V_D = 10 V		
5	SWITCH	$I_{D(on)} + I_{S(on)}$	Channel ON Leakage Current		–2	–2000		–10	–200	nA	V_D = –10 V, I_S = 0		
6	INPUT	I_{INL}	Input Current, Input Voltage Low	–1.0	–0.8	–0.8	–1.0	–0.8	–0.8	mA	V_{IN} = 0 (Sw_1 ON)		
7	INPUT	I_{INH}	Input Current, Input Voltage High	0.1	0.1	10	0.1	0.1	10	µA	V_{IN} = 5.5 V (Sw_2 ON)		
8	DYN	t_{on}	Turn-ON Time		1.0			1.0		µs	See Switching Time Test Circuit		
9	DYN	t_{off}	Turn-OFF Time		1.5			1.5		µs	See Switching Time Test Circuit		
10	DYN	$C_{S(off)}$	Source OFF Capacitance		6 Typ*			6 Typ*			V_S = 0	f = 1 MHz	
11	SUPPLY	I+	Positive Supply Current		3			3.5		mA	V_{IN} = 0		
12	SUPPLY	I–	Negative Supply Current		–3			–3		mA	V_{IN} = 0		
13	SUPPLY	I_R	Reference Supply Current		–0.1			–0.1		mA	V_{IN} = 0		
14	SUPPLY	I+	Positive Supply Current		3			3.5		mA	V_{IN} = 5 V		
15	SUPPLY	I–	Negative Supply Current		–3			–3		mA	V_{IN} = 5 V		
16	SUPPLY	I_R	Reference Supply Current		–1.5			–1.5		mA	V_{IN} = 5 V		

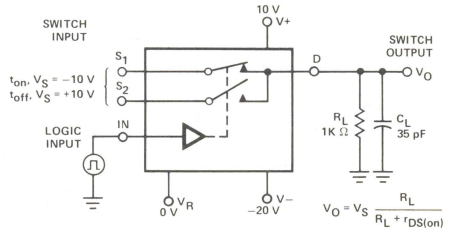
*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

CMBC

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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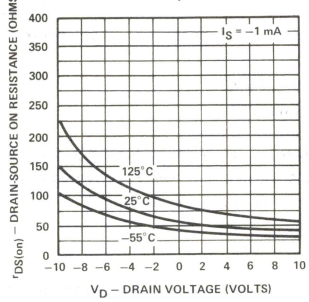
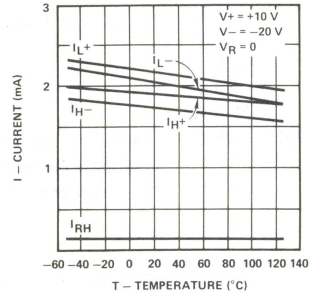
TYPICAL CHARACTERISTICS

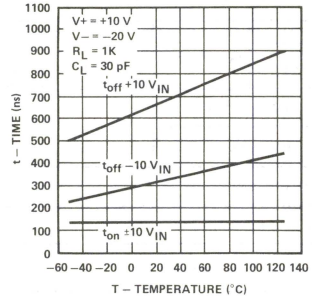
$r_{DS(on)}$ vs V_D and Temperature



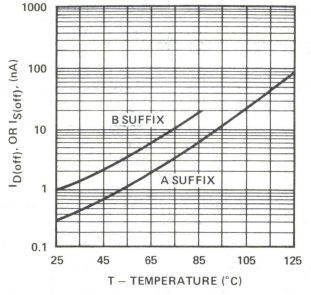
Supply Current vs Temperature



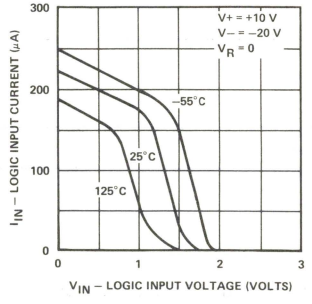
Switching Time vs Temperature



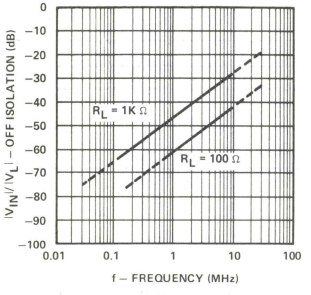
$I_{S(off)}$ vs Temperature



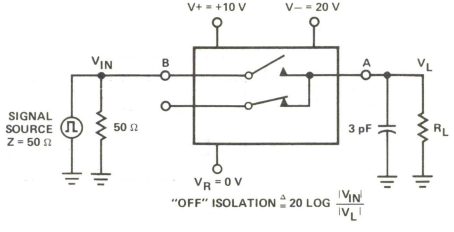
V_{IN} vs I_{IN} and Temperature



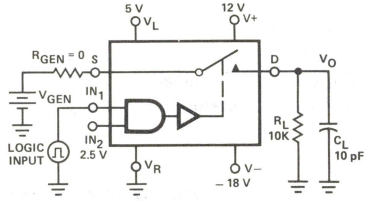
"OFF" Isolation vs R_L and Frequency



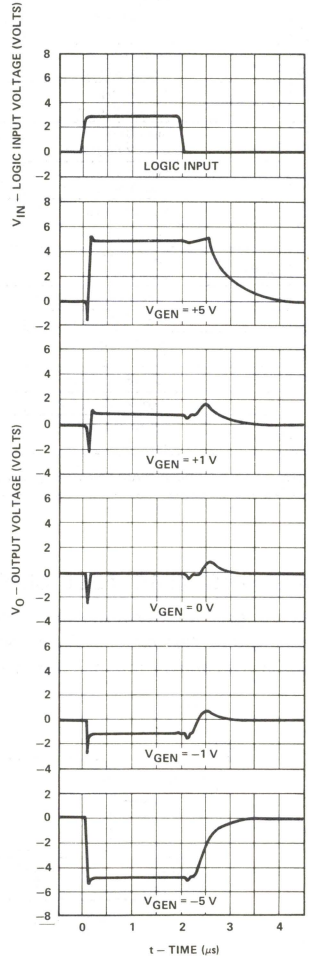
"OFF" Isolation Circuit



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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Monolithic 8-Channel Multiplex Switch with Decode

Siliconix

designed for . . .

■ Multiplexing Analog Signals

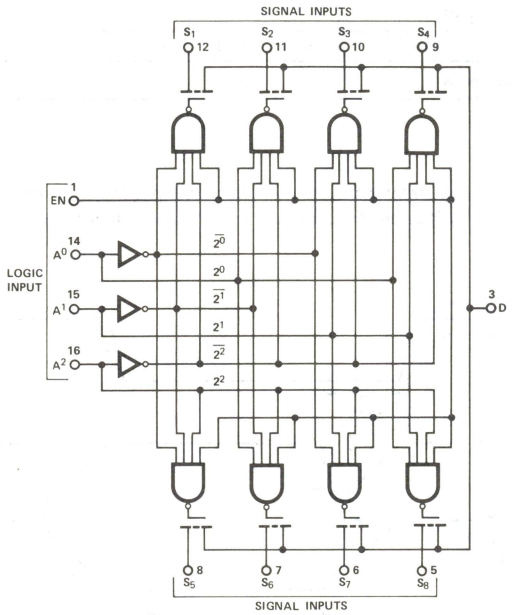
BENEFITS

- **Reduces External Component Requirements**
  - On Board Decoding
  - Internal Zener Diodes Protect MOS Gates
- **Minimizes Channel Cross-Talk Problems**
  - Break-Before-Make Switching

DESCRIPTION

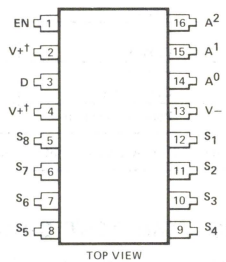
The Si3705 is designed to function as a single-pole, 8-position (plus OFF) electronic switch. The function is implemented by using eight P-channel MOS field-effect transistors as analog switches. In the ON state, each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 5 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word plus an Enable-Inhibit input. The truth table shown below indicates the binary word required to select any one of the eight switch positions. Logic input levels "L" and "H" correspond to positive logic "0" and "1". Assuming supply voltages of +5 and −20 V, logic "L" ≤ 0.6 V and logic "H" ≥ 3.5 V. The rise and fall times of the drivers are designed to provide break-before-make switch action.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS: Si3705142K, Si3705143K, Si3705192K OR Si3705193K
SEE PACKAGE 10

ORDER NUMBER: Si3705192P
SEE PACKAGE 12

†Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

TRUTH TABLE

LOGIC INPUTS				CHANNEL
A^0	A^1	A^2	En	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

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ABSOLUTE MAXIMUM RATINGS

V+ to V−	−0.3, 35 V
V+ to V_A, V_{En}	−0.3, 35 V
V+ to V_D or V_S	−0.3, 35 V
V_D to V_S	±25 V
V_A, V_{En} to V−	35 V
V_D or V_S to V−	35 V

Current (Any Terminal)	−20 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(C Suffix)	0 to 70°C
Power Dissipation*	900 mW

*All leads soldered or welded to PC board. Derate 12 mW/°C above 75°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

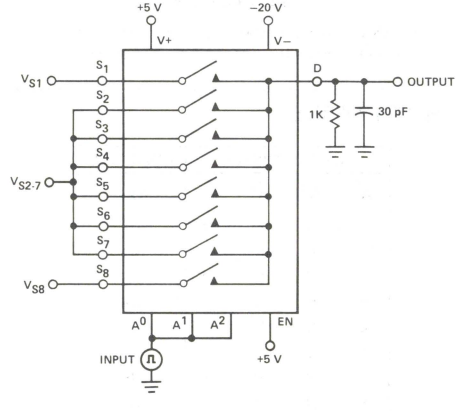
		CHARACTERISTIC		MAX LIMITS SI3705142/SI3705143 −55°C	25°C	85°C	SI3705192/SI3705193 0°C	25°C	70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V− = −20 V, V+ = 5 V, V_{En} = 3.5 V, V_{AL} = 0.6 V, V_{AH} = 3.5 V	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	150	150	225	150	150	200	Ω	V_D = 5 V	I_S = −1 mA
2				200	200	300	200	200	300		V_D = 0	
3				400	400	400	400	400	400		V_D = −5 V −142 and −192 only	
4		$I_{S(off)}$	Source OFF Leakage Current		−1	−100		−3	−150	nA	V_S = −5 V, V_D = 5 V	V_{En} = 0.6 V
5		$I_{D(off)}$	Drain OFF Leakage Current		−8	−500		−10	−500		V_D = −5 V, V_S = 5 V	
6	IN	I_{INL}	Input Current, Input Voltage Low		−1			−1		μA	V_{AL} = 0	
7	DYNAMIC	$t_{transition}$	Switching Time Of Multiplexer		1.5			1.5		μs	See Switching Time Test circuit V_{S1} = ±1 V, V_{S8} = ∓1 V, V_{s2-7} = gnd	
8		t_{on}	Turn-ON Time		1.2 Typ*			1.2 Typ*			See Switching Time Test Circuit $V_{S(all)}$ = 1 V	
9		t_{off}	Turn-OFF Time		0.8 Typ*			0.8 Typ*				
10		t_{open}	Break-Before-Make Interval		0.05 Typ*			0.05 Typ*				
11		$C_{S(off)}$	Source OFF Capacitance		10 Typ*			10 Typ*		pF	V_S = V_D = 5 V	V_{En} = 0.6 V, f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance		20 Typ*			20 Typ*			V_D = 5 V	
13		P_D	Power Dissipation		175			175		mW	V− = −31 V, V+ = 0	

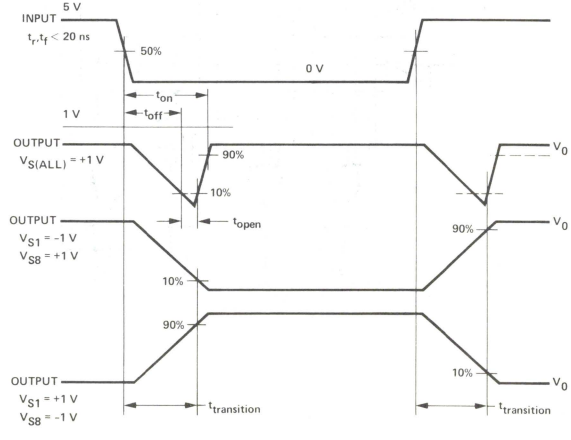
*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

IPAA

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





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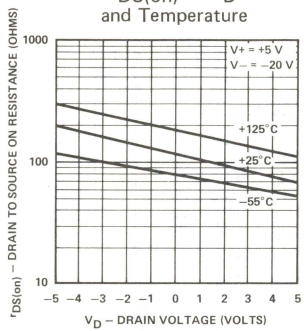
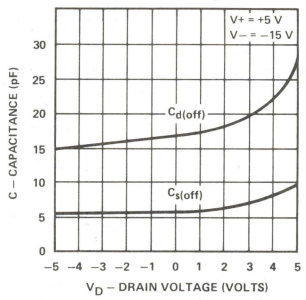
TYPICAL CHARACTERISTICS

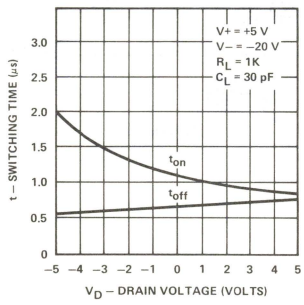
$r_{DS(on)}$ vs V_D and Temperature



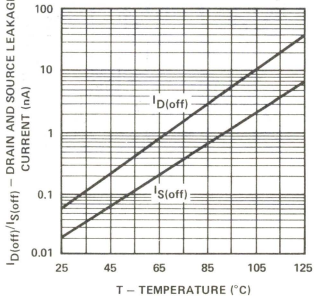
$C_{D(off)}$, $C_{S(off)}$ vs V_D



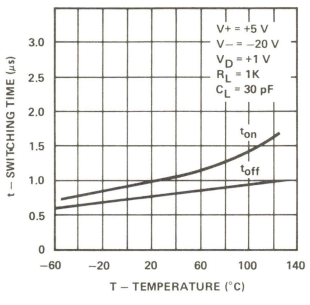
Switching Time vs V_D



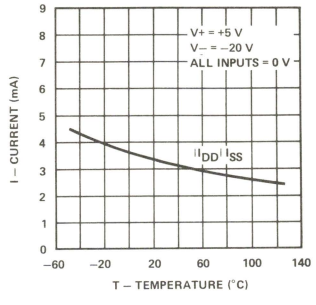
$I_{D(off)}/I_{S(off)}$ vs Temperature



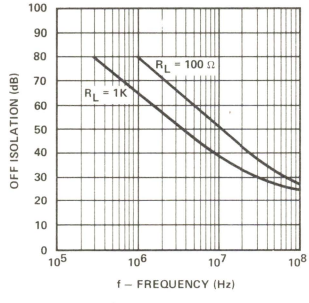
Switching Time vs Temperature

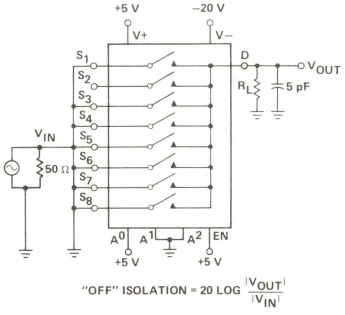


Supply Current vs Temperature

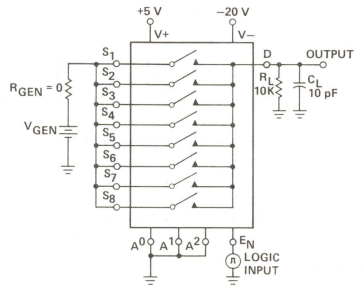


"OFF" Isolation vs R_L and Frequency

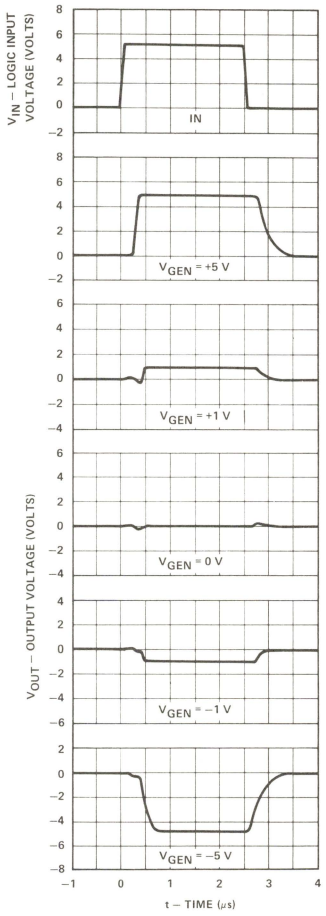




"OFF" ISOLATION = 20 LOG $\frac{|V_{OUT}|}{|V_{IN}|}$



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



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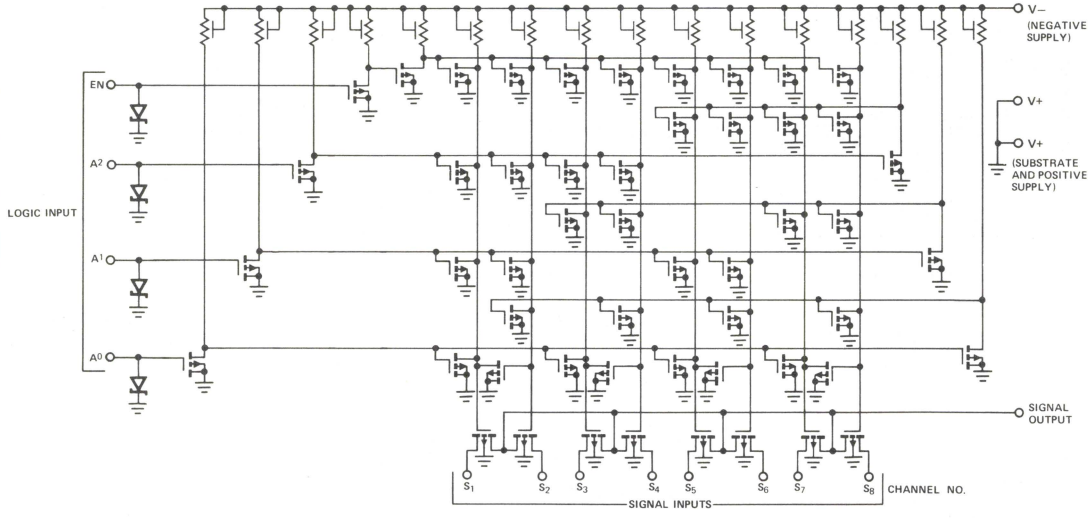
SCHEMATIC DIAGRAM



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Analog Switches 1
Drivers for FET Switches 2
Multi-Channel FETs 3
Die Process and Topography Information 4
Burn-In Pin Connections 5
Mechanical Data 6
Appendices 7

Monolithic 6-Channel FET Switch Drivers

Siliconix

designed for . . .

- **Interfacing Low Level Signals to FET Switches such as G115 and G122 Series Multi-Channel FET Switches**

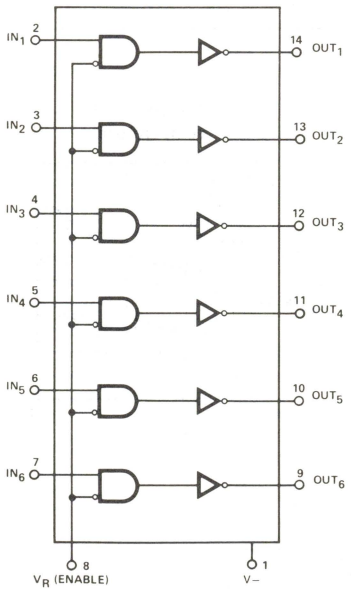
BENEFITS

- **Reduces System Component Requirements**
  - Six Interface Circuits on One Chip
  - Performs Amplification and DC Level Shifting Required Between Low Level Logic and FET Switches

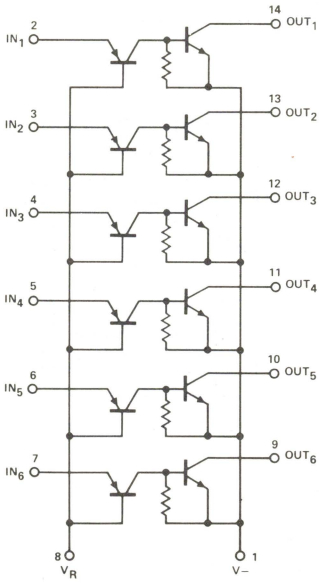
DESCRIPTION

The D123 contains six drivers designed to perform the level-shifting and amplification needed to interface low-level logic outputs and field-effect transistor switches (MOS FET or JFET). With the input logic reference, V_R, at 0 V, the driver output reference, V– may be set between –3 and –30 V. Each output is designed to sink 5 mA of current in the ON condition, and to hold off up to 30 V in the OFF condition. The input stage is a common-base emitter-input PNP transistor, and thus has a low input impedance. For the ON condition, an input current equal to or greater than 1 mA is required.

FUNCTIONAL DIAGRAM

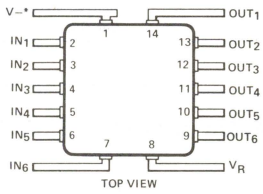


SCHEMATIC DIAGRAM



PIN CONFIGURATIONS

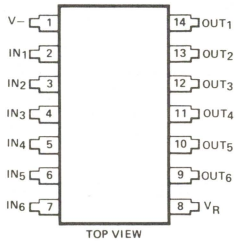
Flat Package



ORDER NUMBER: D123AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

Dual-In-Line Package



ORDER NUMBERS: D123AP OR D123BP
SEE PACKAGE 11

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ABSOLUTE MAXIMUM RATINGS

V_O to V− . . . . . 36 V
V_R to V− . . . . . 25 V
V_{IN} to V− . . . . . 30 V
V_{IN} to V_R . . . . . ±2 V
Current (Any Terminal) . . . . . 30 mA
Storage Temperature . . . . . −65 to 150°C

Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C

Power Dissipation*
Flat Package** . . . . . 750 mW
14 Pin DIP*** . . . . . 825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

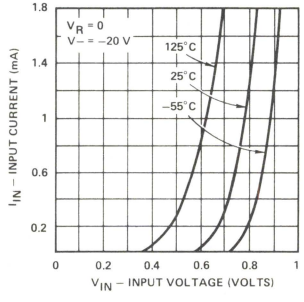
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS D123A −55°C	D123A 25°C	D123A 125°C	D123B −20°C	D123B 25°C	D123B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V− = −20 V, V_R = 0	
1	OUT	V_{OL}	Output Voltage, Low	−19.6	−19.6	−19.5	−19.6	−19.6	−19.5	V	I_O = 5 mA, I_{IN} = 1 mA	
2	OUT	I_{OH}	Output Current, High	0.1	0.1	10	0.1	0.1	10	µA	V_O = 10 V, V_{IN} = 0.4 V	
3	IN	I_{INL}	Input Current, Input Voltage Low	1	1	100	1	1	100	µA	V_{IN} = 0.4 V	
4	IN	V_{INH}	Input Voltage, High	1.3	1	0.8	1.3	1	1	V	I_{IN} = 1 mA	
5	TIME	t_{on}	Turn-ON Time		0.5			0.5		µs	See Switching Time Test Circuit	
6	TIME	t_{off}	Turn-OFF Time		1.2			1.5				
7	SUPPLY	I−	Negative Supply Current	−1	−1	−1.5	−1	−1	−1.5	mA	I_O = 0	I_{IN1} = 1 mA, All Other V_{IN} = 0.4 V
8	SUPPLY	I_R	Reference Supply Current	−0.5	−0.5	−0.5	−0.6	−0.6	−0.6			
9	SUPPLY	I−	Negative Supply Current	−2	−2	−200	−5	−5	−100	µA	V_O = 10 V	All V_{IN} = 0.4 V
10	SUPPLY	I_R	Reference Supply Current	−1	−1	−150	−5	−5	−100			

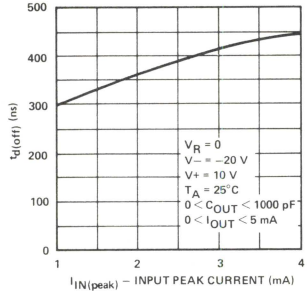
EID

TYPICAL CHARACTERISTICS

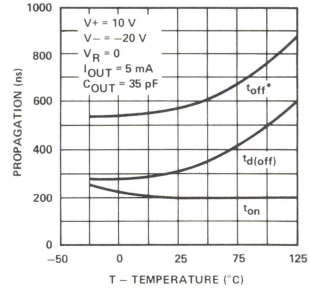
I_{IN} vs V_{IN}



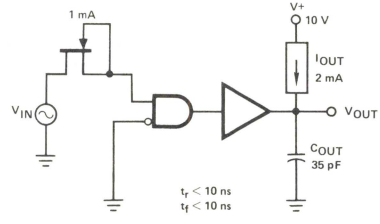
$t_{d(off)}$ vs $I_{IN(PEAK)}$

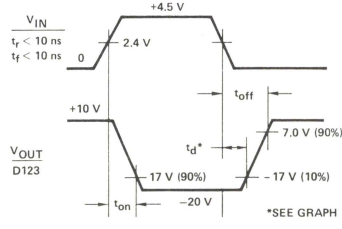


Propagation vs Temperature



SWITCHING TIME TEST CIRCUIT





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Monolithic 6-Channel FET Switch Drivers

Siliconix

designed for . . .

- **Interfacing Low Level Signals to FET Switches such as G115 and G122 Series Multi-Channel FET Switches**

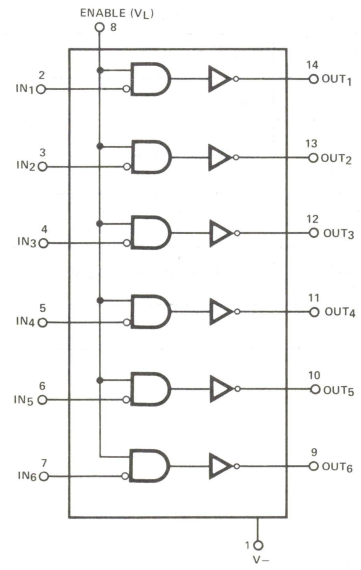
BENEFITS

- **Reduces System Component Requirements**
  - Six Interface Circuits in One Chip
  - Performs Amplification and DC Level Shifting
- **Required Between Low Level Logic and FET Switches**

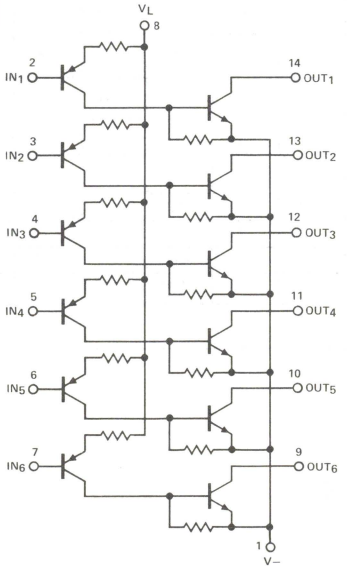
DESCRIPTION

The D125 contains six drivers, designed to perform the level-shifting and amplification needed to interface low-level logic outputs and field-effect transistor switches (MOS FET or JFET). With the input logic supply, V_L, at 5 V, the driver output reference, V– may be set between –1 and –25 V. Each output is designed to sink 5 mA of current in the ON condition, and to hold off up to 30 V in the OFF condition. The input stage is a base-input PNP transistor, with the emitter returned to the V_L supply through a resistor. To turn the driver ON, the logic stage driving it must be capable of sinking 0.7 mA.

FUNCTIONAL DIAGRAM

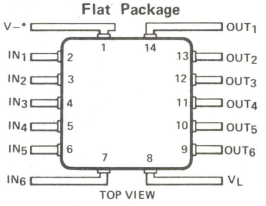


SCHEMATIC DIAGRAM



PIN CONFIGURATIONS

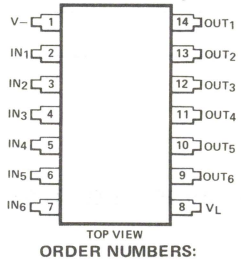
Flat Package



ORDER NUMBER:
D125AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

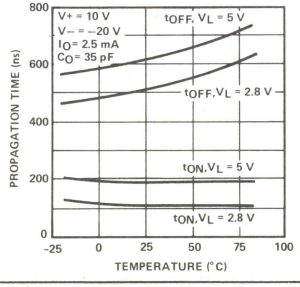
Dual-In-Line Package



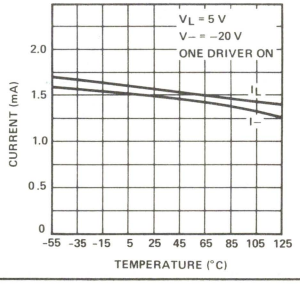
ORDER NUMBERS:
D125AP OR D125BP
SEE PACKAGE 11

TYPICAL CHARACTERISTICS

Propagation vs Temperature



Supply Current vs Temperature



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ABSOLUTE MAXIMUM RATINGS

V_O to V− . . . . . 36 V
V_L to V− . . . . . 30 V
V_{IN} to V− . . . . . 30 V
V_{IN} to V_L . . . . . ±6 V
Current (Any Terminal) . . . . . 30 mA
Storage Temperature . . . . . −65 to 150°C
Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C

Power Dissipation*
Flat Package** . . . . . 750 mW
14 Pin DIP*** . . . . . 825 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C

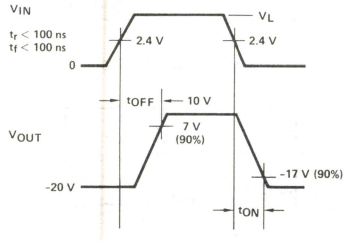
"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

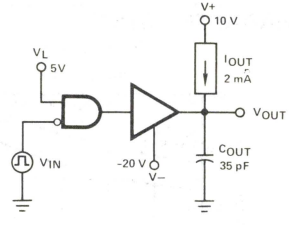
ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS D125A −55°C	D125A 25°C	D125A 125°C	D125B −20°C	D125B 25°C	D125B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V− = −20 V, V_L = 5 V	
1	OUT	V_{OL}	Output Voltage, Low	−19.6	−19.6	−19.5	−19.6	−19.6	−19.5	V	I_O = 5 mA, V_L = 4.5 V, V_{IN} = 0.5 V	
2	OUT	I_{OH}	Output Current, High	0.1	0.1	10	0.1	0.1	10	µA	V_O = 10 V, V_{IN} = 4.6 V	
3	IN	I_{INH}	Input Current, Input Voltage High	±1	±1	±10	±10	±10	±20	µA	V_{IN} = 4.6 V	
4	IN	I_{INL}	Input Current, Input Voltage Low	−0.7	−0.7	−0.7	−1	−1	−1	mA	V_{IN} = 0	
5	TIME	t_{on}	Turn-ON Time		0.5			0.5		µs	See Switching Time Test Circuit	
6	TIME	t_{off}	Turn-OFF Time		1.2			1.5		µs	See Switching Time Test Circuit	
7	SUPPLY	I−	Negative Supply Current	−2.5	−2.5	−2.5	−2.5	−2.5	−2.5	mA	I_O = 0	V_{IN1} = 0, All Other V_{IN} = 4.6 V
8	SUPPLY	I_L	Logic Supply Current	2.5	2.5	2.5	2.5	2.5	2.5	mA	I_O = 0	V_{IN1} = 0, All Other V_{IN} = 4.6 V
9	SUPPLY	I−	Negative Supply Current	−2	−2	−200	−2	−2	−100	µA	V_O = 10 V	All V_{IN} = 4.6 V
10	SUPPLY	I_L	Logic Supply Current	1	1	100	2	2	100	µA	V_O = 10 V	All V_{IN} = 4.6 V
												BID

SWITCHING TIME TEST CIRCUIT





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4-Channel MOS FET Switch Driver with Decode

Siliconix

designed for . . .

- **Interfacing Low Level Signals to FET Switches such as G115 and G123 Series Multi-Channel FET Switches**

BENEFITS

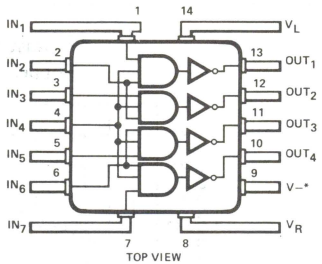
- **Reduces System Component Requirements**
  - Four Interface Circuits in One Chip
- **Easily Interfaced**
  - Inputs Compatible with Low Power TTL and DTL I_F = 200 μA Max
  - Output Current Sinking Capability 10 mA

DESCRIPTION

The D129 is a four-channel driver designed to provide the DC level-shifting and amplification functions needed to interface low-level logic outputs (0.7 to 2.2 V) and field-effect transistor switch inputs (up to 50 V peak-to-peak). With an input logic supply of 5 V, the output transistor emitter, V−, may be set at any voltage between −5 and −30 V. In the ON state, the output collector will sink up to 10 mA of current, and in the OFF state will hold off voltages up to 50 V above V−. Each of the four drivers has a 3-input logic gate, with each of the inputs either open or at positive logic "1", the driver will be ON. With any of the inputs either grounded or at positive logic "0", the driver will be OFF. Some of the logic inputs to the four gates are internally connected to facilitate decoding from a binary counter; however, one input to each gate provides a means for independent operation of each driver, if desired.

PIN CONFIGURATIONS

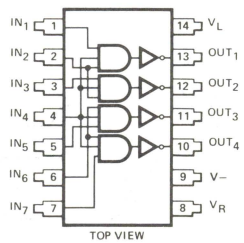
Flat Package



ORDER NUMBER: D129AL
SEE PACKAGE 5

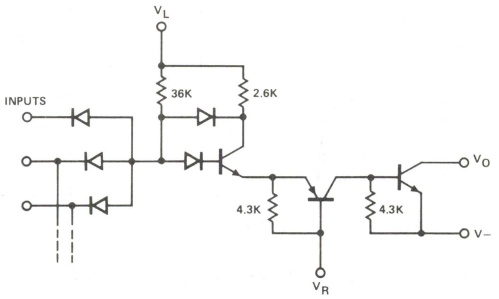
*Common to Substrate and Base of Package

Dual-In-Line Package



ORDER NUMBERS: D129AP OR D129BP
SEE PACKAGE 11

SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

V_O to V− (A Suffix)	50 V
V_O to V− (B Suffix)	36 V
V_R to V− (A Suffix)	33 V
V_R to V− (A Suffix)	24 V
V_L to V_R	8 V
V_{IN} to V_R	±6 V
V_{IN} to V_{IN} (Any Other V_{IN} Terminals)	6 V
Current (Any Terminal)	30 mA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.

**Derate 10 mW/°C above 75°C

***Derate 11 mW/°C above 75°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

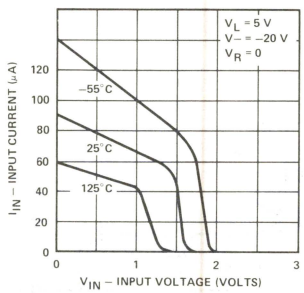
		CHARACTERISTIC		MAX LIMITS D129A −55°C	D129A 25°C	D129A 125°C	D129B −20°C	D129B 25°C	D129B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V− = −20 V, V_R = 0, V_L = 5 V	
1	OUT	V_{OL}	Output Voltage, Low	−19.3	−19.3	−19	−19.25	−19.25	−19	V	I_O = 10 mA	V_{IN} = 2.2 V, V_L = 4.5 V
2	OUT	V_{OL}	Output Voltage, Low	−19.8	−19.8	−19.75				V	I_O = 1 mA	V_{IN} = 2.2 V, V_L = 4.5 V
3	OUT	I_{OH}	Output Current, High	0.1	0.1	20	0.2	0.2	10	µA	V_O = 10 V, V_{IN} = 0.7 V	
4	IN	I_{INH}*	Input Current, Input Voltage High	0.25	0.25	5	1	1.0	5	µA	V_{IN} = 5 V Input Under Test, V_{IN} = 0 All Other Inputs	
5	IN	I_{INL}*	Input Current, Input Voltage Low	−250	−200	−160	−250	−225	−200	µA	V_{IN} = 0, V_L = 5.5 V	
6	TIME	t_{on}	Turn-ON Time		0.25			0.3		µs	See Switching Time Test Circuit	
7	TIME	t_{off}	Turn-OFF Time		1.0			1.5		µs	See Switching Time Test Circuit	
8	SUPPLY	I−	Negative Supply Current		−2			−2.25		mA	V− = −20 V, V_L = 5.5 V	One Channel "ON"
9	SUPPLY	I_L	Logic Supply Current		3			3.3		mA	V− = −20 V, V_L = 5.5 V	One Channel "ON"
10	SUPPLY	I−	Negative Supply Current		−10			−25		µA	V− = −20 V, V_L = 5.5 V	All V_{IN} = 0, All Channels "OFF"
11	SUPPLY	I_L	Logic Supply Current		0.75			1		mA	V− = −20 V, V_L = 5.5 V	All V_{IN} = 0, All Channels "OFF"

*Per gate input

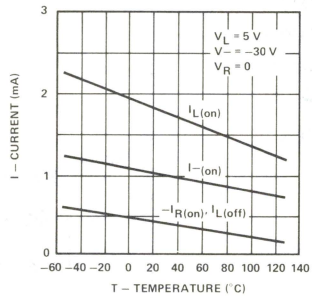
IBAD-A

TYPICAL CHARACTERISTICS

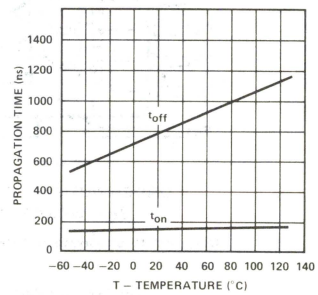
I_{IN} vs V_{IN}



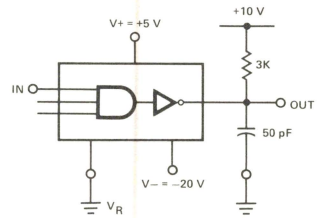
Current vs Temperature

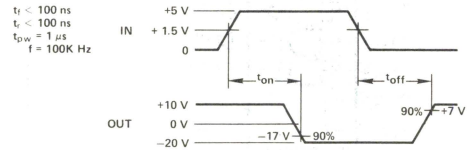


Propagation vs Temperature



SWITCHING TIME AND TEST CIRCUIT





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monolithic 2-channel FET switch driver

Siliconix

designed for . . .

- **Interfacing Low Level Signals to FET Switches**
- **Interfacing TTL to CMOS**
- **Interface from TTL to Other Logic Levels, i.e. PROM Program Levels**

BENEFITS

- **Easily Interfaced**
  - TTL, DTL and RTL Compatible
- **Minimizes Switching Time**
  - 150 ns Typical Propagation Time
- **Versatile**
  - Complementary Outputs
  - Up to 30 V Output Swing

DESCRIPTION

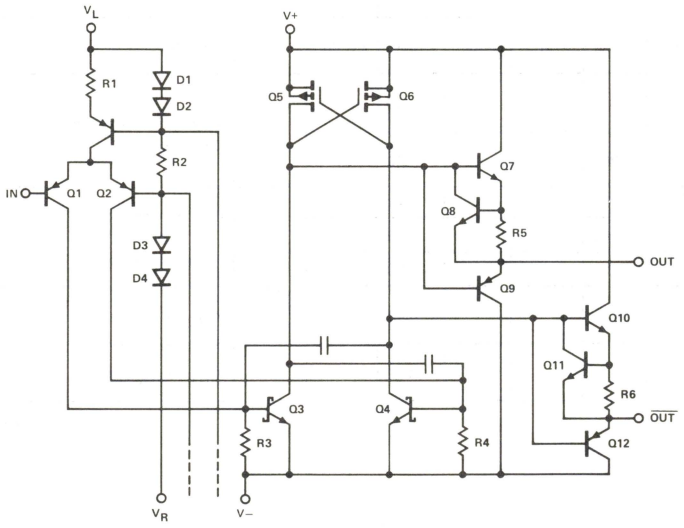
The D139 is a dual low level to high level voltage translator with complementary outputs. Uses include bipolar to MOS logic interface and bipolar logic to FET analog switch control.

The following characteristics of the input circuit provide an ideal interface to the common logic forms TTL, CMOS, and DTL: light loading (≈ 1/3 TTL load) to "0" inputs, a 1.2 V trip point, and high input impedance with high breakdown to "1" inputs.

The output can drive up to 30 V peak-to-peak into pure capacitive loads or moderate resistive loads. Current source coupling between the input and output and split power supplies allow wide flexibility in the actual output voltage levels. Complementary outputs permit maximum application versatility, allowing functions such as double-throw analog switch control.

A positive logic "1" at the input provides a "1" at OUT and a "0" at $\overline{\text{OUT}}$.

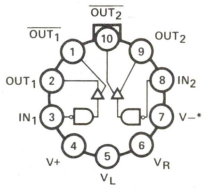
SCHEMATIC DIAGRAM (Typical Channel)



Logic	OUT	$\overline{\text{OUT}}$
0	V−	V+
1	V+	V−

PIN CONFIGURATIONS

Metal Can Package

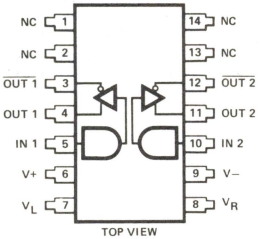


TOP VIEW

*COMMON TO SUBSTRATE AND CASE

ORDER NUMBERS
D139AA or D139BA
SEE PACKAGE 2

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS D139AP
OR D139BP
SEE PACKAGE 11
ORDER NUMBER D139CJ
SEE PACKAGE 7

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ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_R	36 V
V+ to V_O	36 V
V_L to V_R	8 V
V_{IN} to V_R	8 V
V_R to V−	36 V
V_L to V−	36 V
V_O to V−	36 V
V_L to V_{IN}	8 V
Current (Any Terminal) DC	12 mA
Peak (Any Terminal) (200 μs pulse width, 100 pps)	100 mA
Operating Temperature	
(A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
(C Suffix)	0 to 70°C
Storage Temperature	
(A & B Suffix)	−65 to 150°C
(C Suffix)	−65 to 125°C
Power Dissipation (L Package)*	750 mW
(P Package)*	825 mW
(J Package)*	470 mW
Thermal Resistance (θ_{JA}, J Package)	0.16°C/W

*All leads soldered or welded to PC board.
Derate L package 10 mW/°C above 75°C
Derate P package 11 mW/°C above 75°C
Derate J package 6.5 mW/°C above 25°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

	CHARACTERISTIC		D139AA/AP (MIN)/MAX LIMITS			D139BA/BP (D139CJ) (MIN)/MAX LIMITS			UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V_L = 5 V, V− = −20 V, V_R = 0	
			−55°C	25°C	125°C	−20°C (0°C)	25°C	85°C (70°C)			
1	$V_{OH}/V_{\overline{OH}}$	Output Voltage, High (V+ to V_O)	1.1	0.9	0.7	1.1	0.9	0.7	V	I_{OUT} = −10 μA	V_{IH} = 2 V for $V_{OH}/V_{\overline{OL}}$, V_{IL} = 0.8V for $V_{\overline{OH}}/V_{OL}$
2			1.5	1.5	1.5	1.5	1.5	1.5		I_{OUT} = −2 mA	
3	$V_{OL}/V_{\overline{OL}}$	Output Voltage, Low (V_O to V−)	1.3	1.1	0.9	1.3	1.1	0.9		I_{OUT} = 10 μA	
4			1.5	1.5	1.5	1.5	1.5	1.5		I_{OUT} = 2 mA	
5	I_{INH}	Input Current, Input Voltage High		10	20		10	20	μA	V_{IN} = 5 V	
6	I_{INL}	Input Current, Input Voltage Low	(−600)	(−500)	(−500)	(−600)	(−500)	(−500)		V_{IN} = 0	
7	$t_{(+)}$	Switching Time, Low to High, Delay Plus Rise Time		170			170		ns	See Switching Time Test Circuit (C_L = 35 pF)	
8	$t_{(-)}$	Switching Time, High to Low, Delay Plus Fall Time		200			200				
9	I+	Positive Supply Current		0.1			0.1		mA	Input Voltage High or Input Voltage Low	
10	I_L	Logic Supply Current		4.0			4.0				
11	I−	Negative Supply Current		−3.0			−3.0				
12	I_{RH}	Reference Supply Current Input Voltage High		(−1.6)			(−1.6)			V_{IN1} = V_{IN2} = 5 V	
13	I_{RL}	Reference Supply Current, Input Voltage Low		(−1.1)			(−1.1)			V_{IN1} = V_{IN2} = 0 V	

CMO

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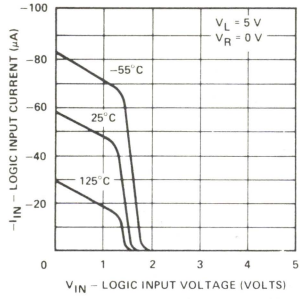
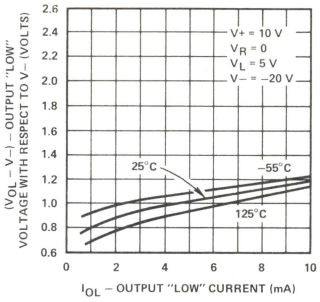
TYPICAL CHARACTERISTICS

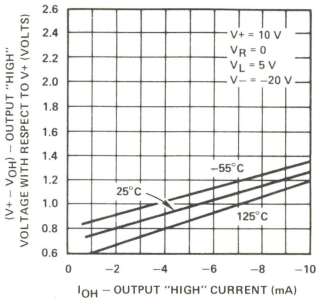
Logic Input Current vs Logic Input Voltage



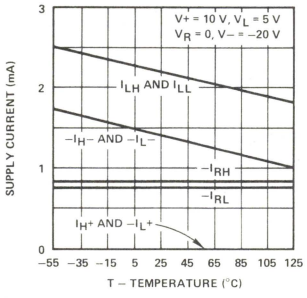
Output "Low" Characteristic



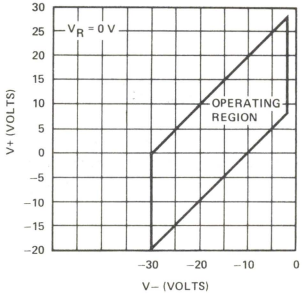
Output "High" Characteristic



Supply Current vs Temperature



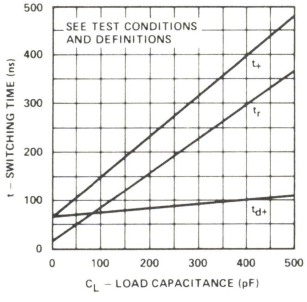
Selecting V+ and V−



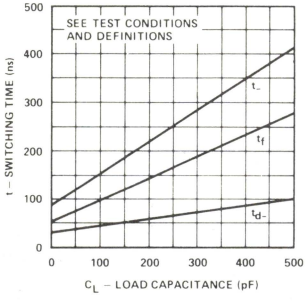
Selecting V+ and V−

The output swings between V+ and V− ($V_{OH} \cong$ V+ and $V_{OL} \cong$ V−). Select V+ and V−, within the operating region of curve at left, to provide the desired output swing. Note that V− can be −2.0 V to −30 V and V+ − V− must be at least 10 V.

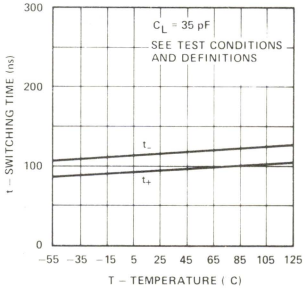
Switching Time, Low to High, vs Load Capacitance



Switching Time, High to Low, vs Load Capacitance

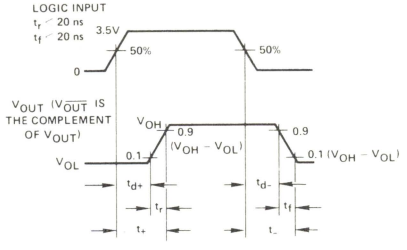


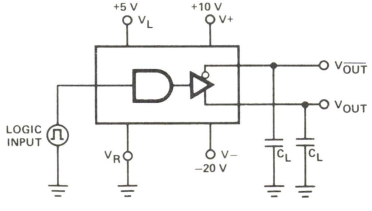
Switching Time vs Temperature



TEST CONDITIONS AND DEFINITIONS

Switching Time Test Circuit





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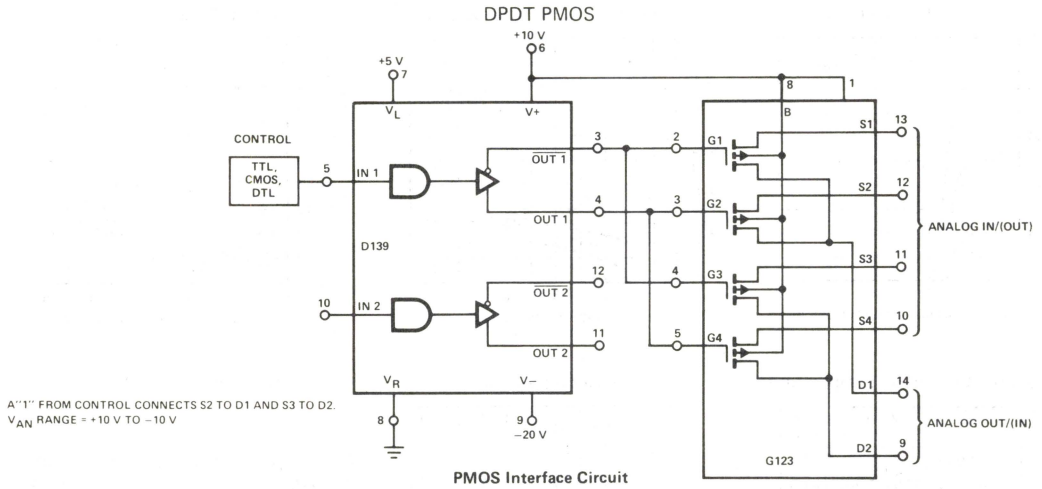
DRIVING PMOS ANALOG SWITCHES



PMOS Interface Circuit
Figure 1

Driving PMOS Analog Switches. The D139 output swing is dictated by the analog signal range. V_{OH} is the PMOS "OFF" level and must equal the most positive analog voltage. V_{OL} is the PMOS "ON" level and must be 10 V more negative than the most negative analog voltage. Therefore for $V_{AN} = \pm 10$ V → V+ = +10 V and V− = −20 V. PMOS control is make-before-break.

PMOS LOGIC INTERFACE

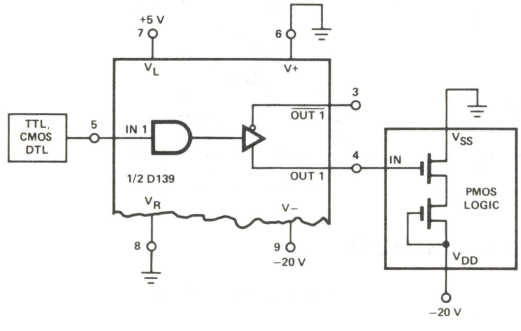


Figure 2

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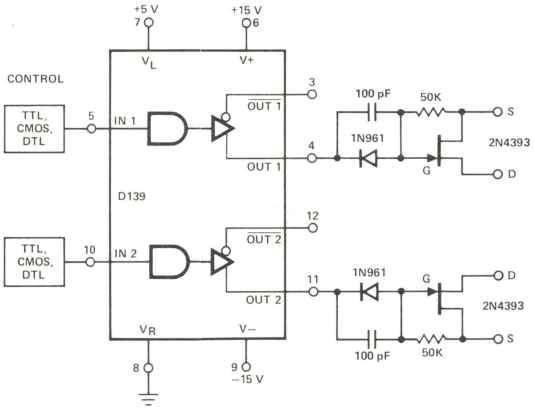
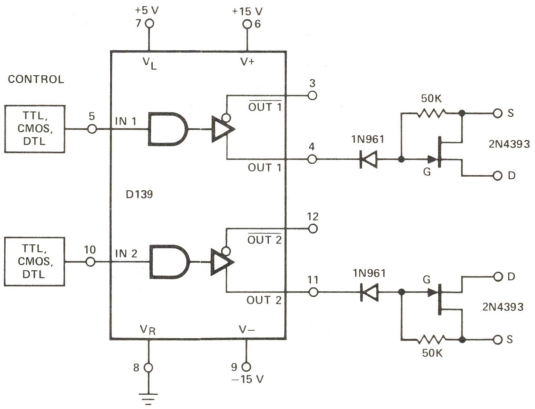
DRIVING NJFET ANALOG SWITCHES

Fast Dual SPST, NJFET, for Low Frequency Signals (1)



THE 2N4393 WILL BE "ON" FOR A "1" FROM CONTROL.
V_{AN} RANGE = +10 V TO −10 V.

Dual SPST, NJFET for High Frequency Signals (1)



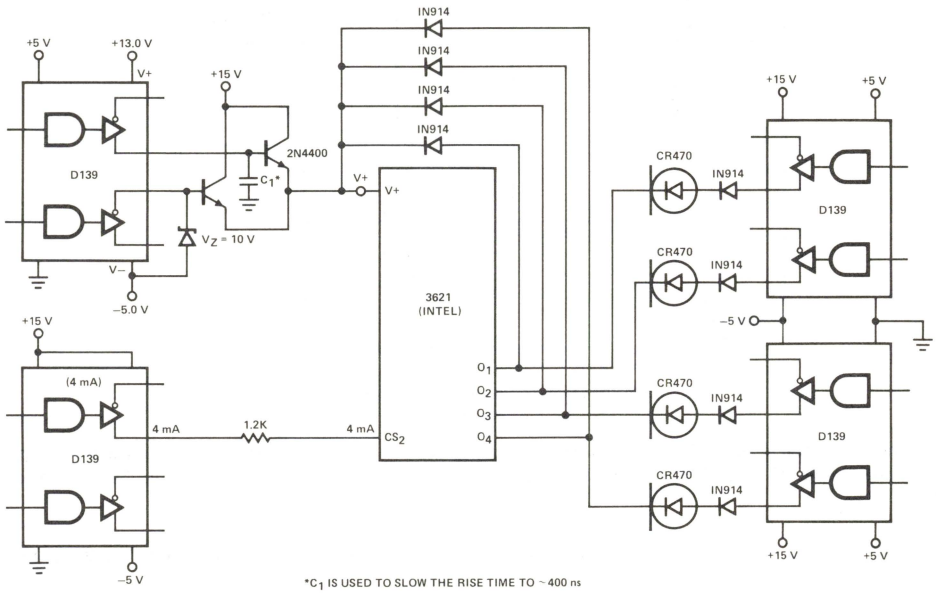
THE 2N4393 WILL BE "ON" FOR A "1" FROM CONTROL.
V_{AN} RANGE = +10 V TO −10 V.

Figure 3

Driving NJFET Analog Switches. V_{OH} is the "ON" NJFET level and must be isolated from the gate by a series diode as shown above to prevent forward gate current. V_{OL} is the "OFF" NJFET level and must be more negative than the most negative analog signal voltage by ($|V_{GS(off)}|$ +2 V). NJFET control is break-before-make.

(1) See Siliconix Application Note "Driver Circuits for the J-FET Analog Switch" AN73-5, August 1973.

APPLICATIONS



D139 Used in Programming the Intel 3621 PROM
Figure 4

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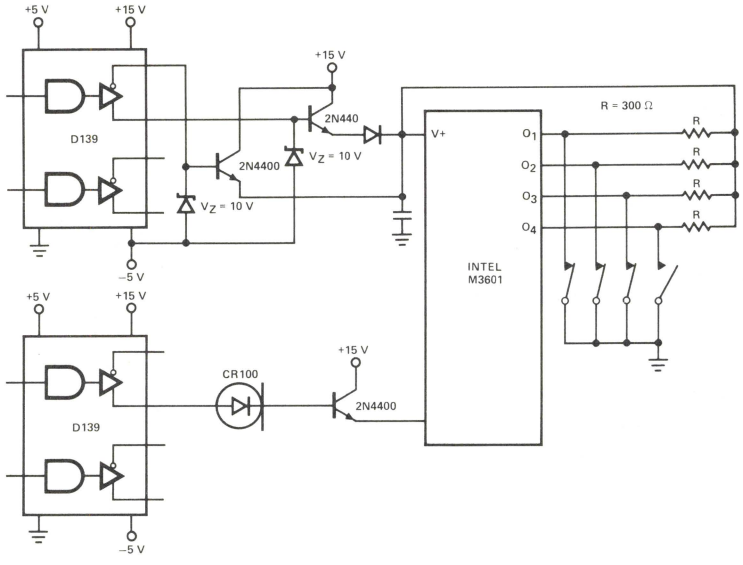
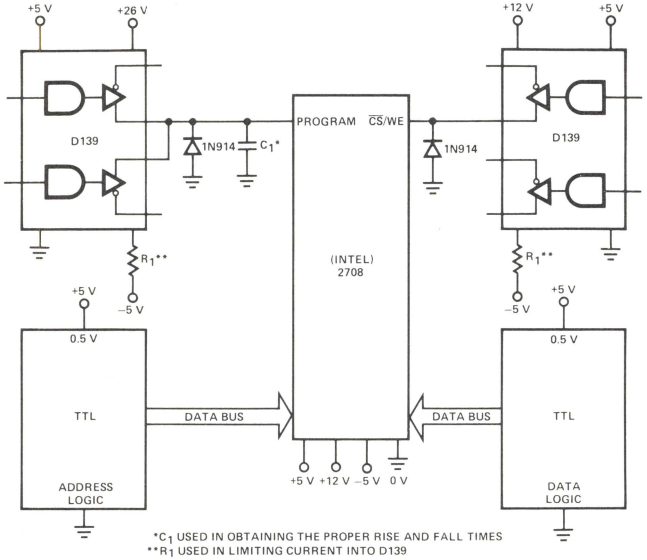
APPLICATIONS (Cont'd)



D139 Used in Programming the Intel 3601 PROM
Figure 5



D139 Used in Programming the Intel 2708 PROM
Figure 6

D139 2-Channel Interface. The D139 may be used to interface 0.5 V TTL to CMOS Logic by setting V_L, V_R, V+ and V− to the proper levels. If 0 to 5 V TTL levels are to be used to control the switch, V_L should be set to 5 V and V_R grounded.

V+ and V− may be set to whatever levels are needed. The operating region of the D139 is determined by the graph of V+ vs V−.

Note. V− must be at least 2 V below V_R in order for the D139 to operate. See the V+ vs V− graph for selecting the supply voltages within the operating region.

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Analog Switches 1
Drivers for FET Switches 2
Multi-Channel FETs 3
Die Process and Topography Information 4
Burn-In Pin Connections 5
Mechanical Data 6
Appendices 7

Monolithic 6-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing**

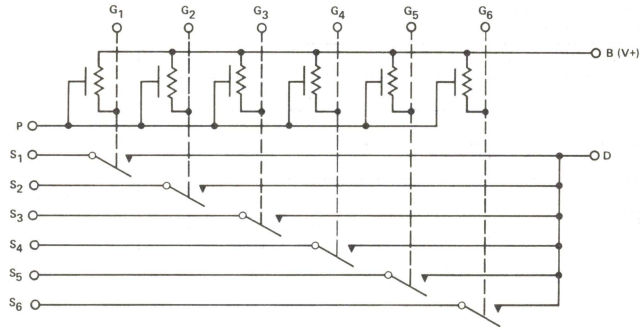
BENEFITS

- **Reduces External Component Requirements**
  - Internal Zener Diode Protects the Gate
  - Six Switches Per Chip
  - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

DESCRIPTION

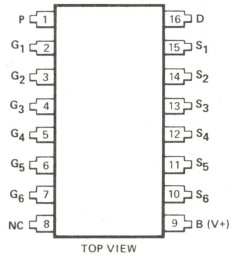
The G115 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated on a silicon substrate (body). The switches have a common drain terminal (D) which will function equally well as a common source. In the same manner, the source terminals (S) will function equally well as drains. Each gate (G) is provided with a normally OFF "pull-up" MOS FET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

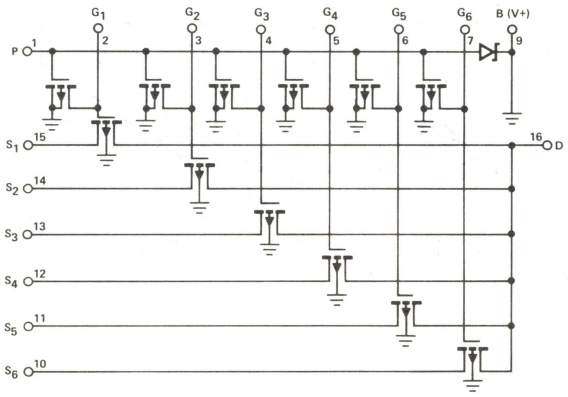
Dual-In-Line Package



TOP VIEW

ORDER NUMBERS: G115AP OR G115BP
SEE PACKAGE 12

SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

V_B to V_S . . . . . −2 to 30 V
V_B to V_D . . . . . −2 to 30 V
V_D to V_S . . . . . ±30 V
V_B to V_G, V_B to V_P . . . . . 35 V
I_S, I_D . . . . . 100 mA
I_G . . . . . 5 mA
I_P . . . . . 100 μA

Storage Temperature . . . . . −65 to 150°C
Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
Power Dissipation* . . . . . 900 mW

*All leads soldered or welded to PC board. Derate 12 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

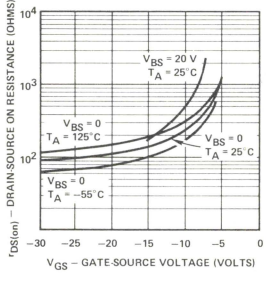
		CHARACTERISTIC		MAX LIMITS G115A −55°C	G115A 25°C	G115A 125°C	G115B −20°C	G115B 25°C	G115B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0		
1		$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V	I_S = −1 mA	
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V		
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4		$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−2.5	−2500		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6	STATIC	$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V		
7		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V		
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{DG} = 0, V_{SB} = 0		
9		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0		
10		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA		
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0		
13	DYNAMIC	C_{gs}	Gate-Source Capacitance		0.9 Typ*			0.9 Typ*		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
14		C_{gd}	Gate-Drain Capacitance		0.9 Typ*			0.9 Typ*				Source Guarded	
15		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
16		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
17		C_{db}	Drain-Body Capacitance		12 Typ*			12 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

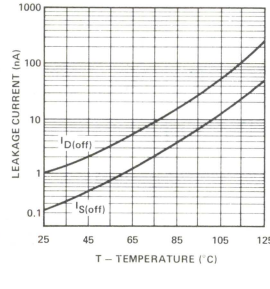
MAB-A

TYPICAL CHARACTERISTICS

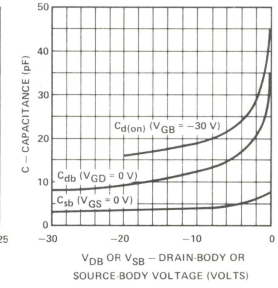
$r_{DS(on)}$ vs V_{GS}



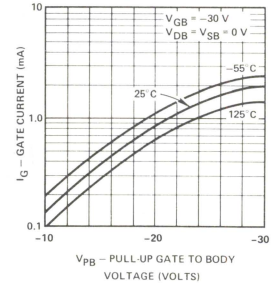
$I_{S(off)}$, $I_{D(off)}$ vs Temperature



Capacitance vs V_{DB} or V_{SB}



I_G vs V_{PB}



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Monolithic 5-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing**

BENEFITS

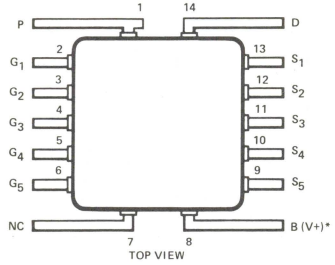
- **Reduces External Component Requirements**
  - Internal Zener Diode Protects the Gate
  - Five Switches Per Chip
  - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

DESCRIPTION

The G116 contains five enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated on a silicon substrate (body). The switches have a common drain terminal (D) which will function equally well as a common source. In the same manner, the source terminals (S) will function equally well as drains. Each gate (G) is provided with a normally OFF "pull-up" MOS FET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively. It is recommended that the G115 be used for new designs.

PIN CONFIGURATIONS

Flat Package

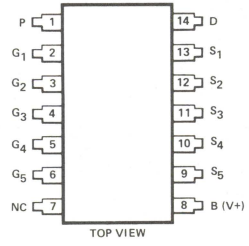


TOP VIEW

ORDER NUMBER: G116AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

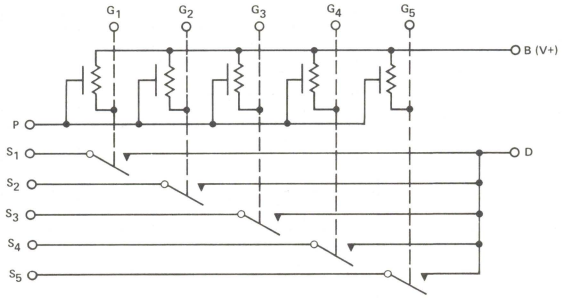
Dual-In-Line Package



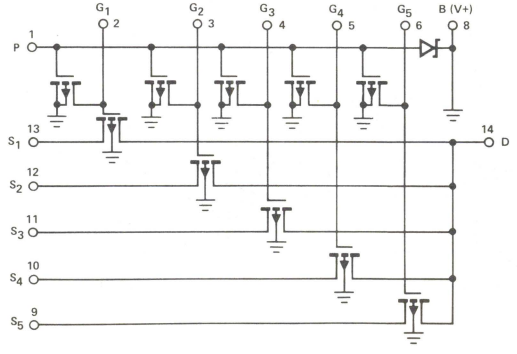
TOP VIEW

ORDER NUMBER: G116AP
SEE PACKAGE 11

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

V_B to V_S	−2 to 30 V
V_B to V_D	−2 to 30 V
V_D to V_S	±30 V
V_B to V_G, V_B to V_P	35 V
I_S, I_D	100 mA
I_G	5 mA
I_P	100 μA
Storage Temperature	−65 to 150°C
Operating Temperature	−55 to 125°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

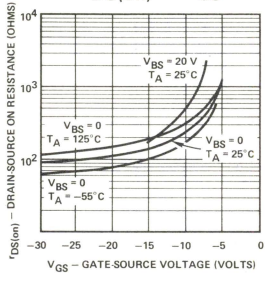
		CHARACTERISTIC		MAX LIMITS G116A −55°C	G116A 25°C	G116A 125°C	G116B −20°C	G116B 25°C	G116B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0		
1		$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V	I_S = −1 mA	
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V		
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4		$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−2.5	−2500		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6	STATIC	$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V		
7		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V		
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.4 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{SB} = 0, V_{DG} = 0		
9		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0		
10		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA		
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0		
13		C_{gs}	Gate-Source Capacitance		0.9 Typ*			0.9 Typ*		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
14	DYNAMIC	C_{gd}	Gate-Drain Capacitance		0.9 Typ*			0.9 Typ*				Source Guarded	
15		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
16		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
17		C_{db}	Drain-Body Capacitance		12 Typ*			12 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

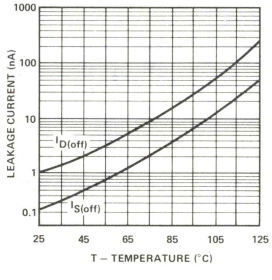
MAB-A

TYPICAL CHARACTERISTICS

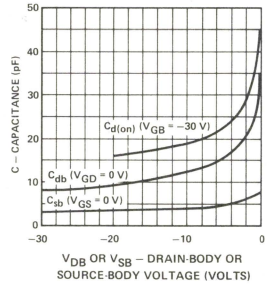
$r_{DS(on)}$ vs V_{GS}



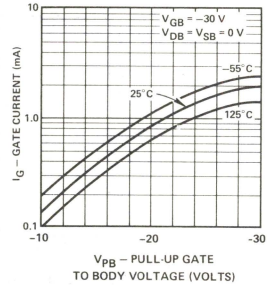
$I_{S(off)}$, $I_{D(off)}$ vs Temperature



Capacitance vs V_{DB} or V_{SB}



I_G vs V_{PB}



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Monolithic 5-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing with Enable Switch**

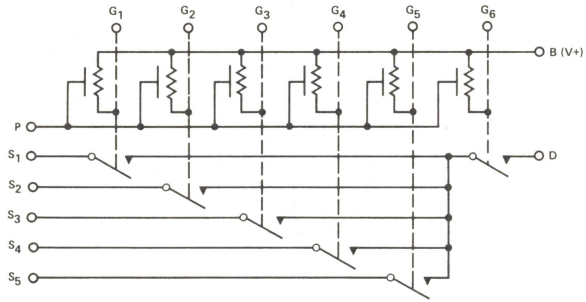
BENEFITS

- **Reduces External Component Requirements**
  - Internal Zener Diode Protects the Gate
  - Five Switches Per Chip
  - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

DESCRIPTION

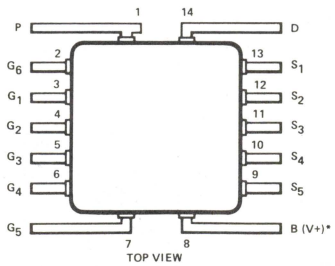
The G117 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The switches are integrated on a silicon substrate (body). The drains of five of the switches are internally connected to the source of the sixth switch. This arrangement is intended for use of the device as a 5-channel first-level and one-channel second-level multiplexer. Each of the six gates are provided with an internal "pull-up" current which may be turned ON or OFF by connecting the pull-up control terminal (P) to a negative supply or to the body (B) terminal.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

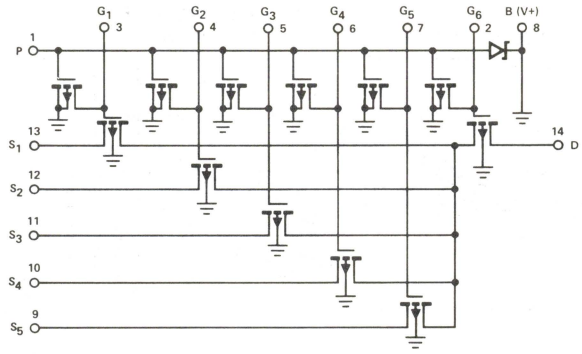
Flat Package



ORDER NUMBER: G117AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

V_B to V_S . . . . . −2 to 30 V
V_B to V_D . . . . . −2 to 30 V
V_D to V_S . . . . . ±30 V
V_B to V_G, V_B to V_P . . . . . 35 V
I_S, I_D . . . . . 100 mA
I_G . . . . . 5 mA
I_P . . . . . 100 μA

Storage Temperature . . . . . −65 to 150°C
Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
Power Dissipation* . . . . . 750 mW
*All leads soldered or welded to PC board. Derate 10 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

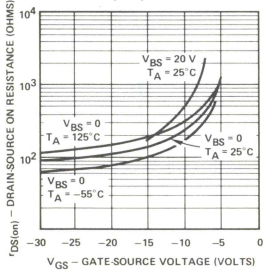
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS G117A −55°C	G117A 25°C	G117A 125°C	G117B −20°C	G117B 25°C	G117B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0	
1		$r_{DS(on)}$*	Drain-Source ON Capacitance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V	I_S = −1 mA, V_{G6D} = V_{GD}
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V	
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−10	nA	V_{SD} = −20 V, V_{GD} = 0	
5		$I_{D(off)}$	Drain OFF Leakage Current		−2.5	−2500		−10	−500		V_{DS} = −20 V, V_{GS} = 0, V_{G6S} = −30 V, V_{SB} = 0	
6	STATIC	$I_{D(off)}$	Drain OFF Leakage Current		−0.5	−500		−5	−100		V_{DS} = −20 V, V_{GS} = −30 V, V_{G6B} = 0, V_{SB} = 0	
7		$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{DB} = −30 V	
8		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V	
9		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_S = 10 μA, V_{DG1-5} = 0, V_{GB6} = −20 V	
10		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0		I_{S1} = 10 μA, V_{DG6} = 0, V_{GB1} = −20 V	
11		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0	
12		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0	
13		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA	
14		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0	
15		C_{gs}	Gate-Source Capacitance		0.9 Typ**			0.9 Typ**		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded; V_{GB} = 0, f = 1 MHz
16	DYNAMIC	C_{gd}	Gate-Drain Capacitance		0.9 Typ**			0.9 Typ**				Source Guarded
17		$C_{ds(off)}$*	Drain-Source OFF Capacitance		0.4 Typ**			0.4 Typ**				Gate Guarded
18		C_{sb}	Source-Body Capacitance		2 Typ**			2 Typ**			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded
19		C_{db}	Drain-Body Capacitance		12 Typ**			12 Typ**			$V_{S(1-5)B}$ = 0, $V_{G(1-5)B}$ = 0, V_{G6B} = −30 V, V_{DB} = −5 V, All Gates and Sources Guarded	

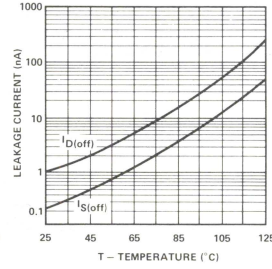
*This is resistance (capacitance) from each source to common internal node. Multiply resistance by two for total resistance from inputs to output. MAB
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

TYPICAL CHARACTERISTICS

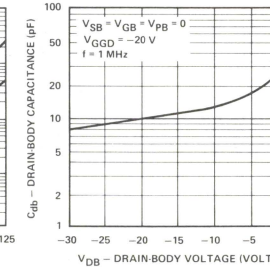
$r_{DS(on)}$ vs V_{GS}



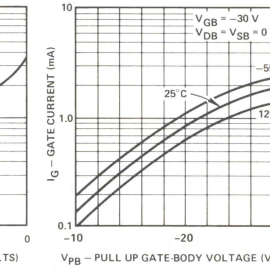
$I_{S(off)}$, $I_{D(off)}$ vs Temperature



C_d vs V_{DB}



I_G vs V_{PB}



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Monolithic 6-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing**

BENEFITS

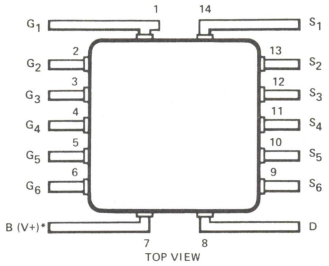
- **Reduces External Component Requirements**
  - Internal Zener Diode Protects the Gate
  - Six Switches Per Chip

DESCRIPTION

The G118 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The switches are integrated on a common substrate (body). They have a common drain terminal (D) which will function equally well as a common source; likewise, the source terminals will function as drains.

PIN CONFIGURATIONS

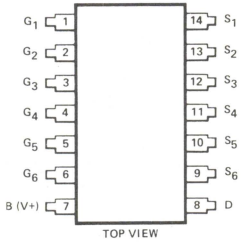
Flat Package



ORDER NUMBER: G118AL
SEE PACKAGE 5

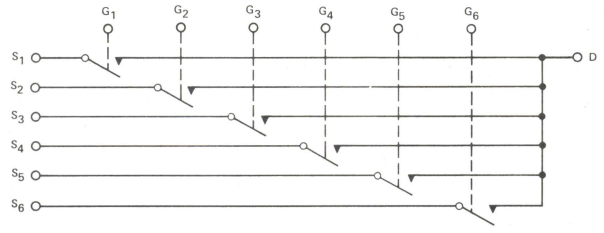
*Common to Substrate and Base of Package

Dual-In-Line Package

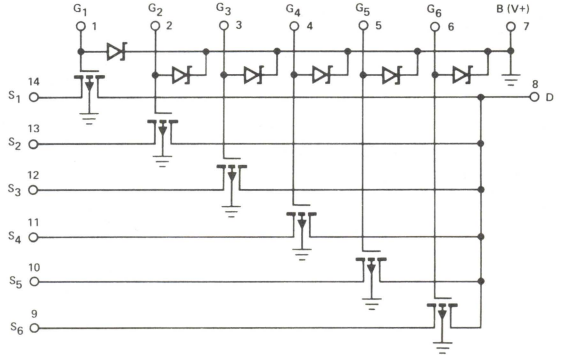


ORDER NUMBER: G118AP
SEE PACKAGE 11

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

V_B to V_S . . . . . −2 to 30 V
V_B to V_D . . . . . −2 to 30 V
V_D to V_S . . . . . ±30 V
V_B to V_G . . . . . 35 V
I_S, I_D . . . . . 100 mA
I_G . . . . . 5 mA
Storage Temperature . . . . . −65 to 150°C
Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C

Power Dissipation*
Flat Package** . . . . . 750 mW
14 Pin DIP*** . . . . . 825 mW

*All leads soldered or welded to PC board.
**Derate 10 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

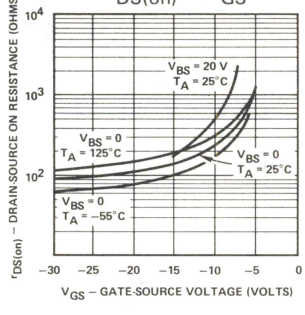
		CHARACTERISTIC		MAX LIMITS G118A −55°C	G118A 25°C	G118A 125°C	G118B −20°C	G118B 25°C	G118B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0		
1		$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V		
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V	I_S = −1 mA	
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4	STATIC	$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−3	−3000		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500		V_{GB} = −20 V		
7		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{GD} = 0, V_{SB} = 0		
8		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0		
9		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
10		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA		
11	DYNAMIC	C_{gs}	Gate-Source Capacitance		0.9 Typ*			0.9 Typ*		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
12		C_{gd}	Gate-Drain Capacitance		0.9 Typ*			0.9 Typ*				Source Guarded	
13		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
14		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
15		C_{db}	Drain-Body Capacitance		12 Typ*			12 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

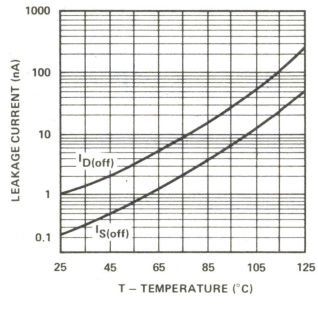
MABA

TYPICAL CHARACTERISTICS

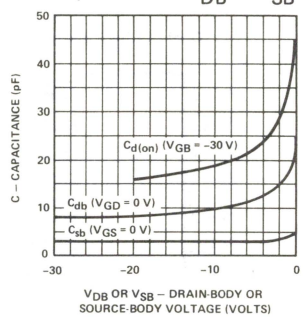
$r_{DS(on)}$ vs V_{GS}



$I_{S(off)}$, $I_{D(off)}$ vs Temperature



Capacitance vs V_{DB} or V_{SB}



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Monolithic 6-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals such as Differential Inputs**
- **Multiplexing**

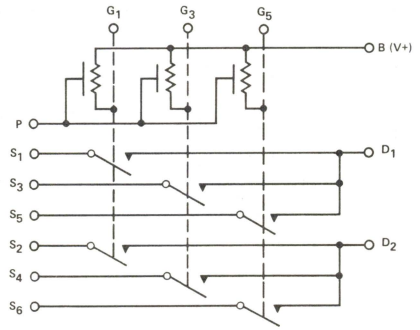
BENEFITS

- **Reduces External Component Requirements**
  - Internal Zener Diode Protects the Gate
  - Six Switches Per Chip
  - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

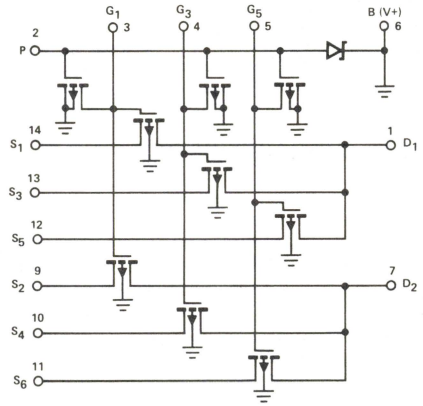
DESCRIPTION

The G119 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated onto a silicon substrate (body) and are internally connected into two groups of three switches per group. This arrangement facilitates the switching or multiplexing of differential analog signals. Each group has a common drain terminal (D_1 and D_2) which will function equally well as a common source. Each gate terminal (G) controls a pair of switches and is provided with a normally-OFF "pull-up" MOS FET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

FUNCTIONAL DIAGRAM



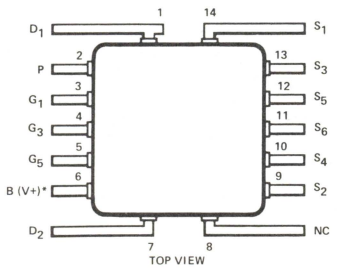
SCHEMATIC DIAGRAM



PIN CONFIGURATION

Flat Package

PIN CONFIGURATION



ORDER NUMBER: G119AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

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ABSOLUTE MAXIMUM RATINGS

V_B to V_S . . . . . −2 to 30 V
V_B to V_D . . . . . −2 to 30 V
V_D to V_S . . . . . ±30 V
V_B to V_G, V_B to V_P . . . . . 35 V
I_S, I_D . . . . . 100 mA
I_G . . . . . 5 mA
I_P . . . . . 100 μA
Storage Temperature . . . . . −65 to 150°C
Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
Power Dissipation* . . . . . 750 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

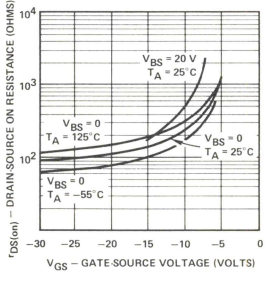
		CHARACTERISTIC		MAX LIMITS G119A −55°C	MAX LIMITS G119A 25°C	MAX LIMITS G119A 125°C	MAX LIMITS G119B −20°C	MAX LIMITS G119B 25°C	MAX LIMITS G119B 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0		
1		$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V		I_S = −1 mA
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V		
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4	STATIC	$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−1.5	−1500		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6		$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V		
7		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V		
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{SB} = 0, V_{GD} = 0		
9		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −50 μA, V_{GS} = 0, V_{SB} = 0		
10	SUPPLY	BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA		
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0		
13		C_{gs}	Gate-Source Capacitance		1.8 Typ*			1.8 Typ*		pF	V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
14	DYNAMIC	C_{gd}	Gate-Drain Capacitance		1.8 Typ*			1.8 Typ*				Source Guarded	
15		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
16		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
17		C_{db}	Drain-Body Capacitance		6 Typ*			6 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

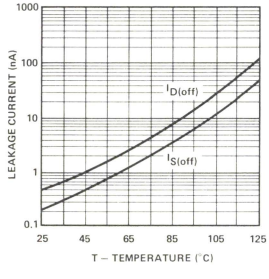
MABB

TYPICAL CHARACTERISTICS

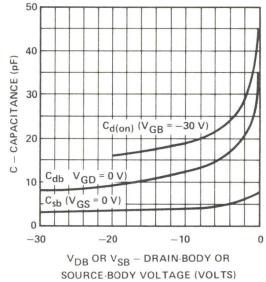
$r_{DS(on)}$ vs V_{GS}



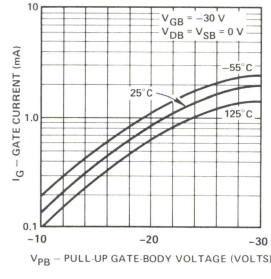
$I_{S(off)}$, $I_{D(off)}$ vs Temperature



Capacitance vs V_{DB} or V_{SB}



I_G vs V_{PB}



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Monolithic 4-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals such as Differential Inputs**
- **Multiplexing**

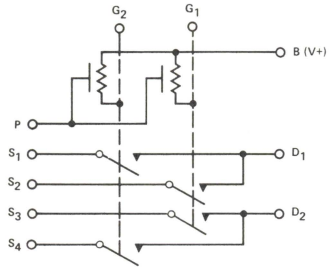
BENEFITS

- **Reduces External Component Requirements**
  - Internal Zener Diode Protects the Gate
  - Four Switches Per Chip
  - Integrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

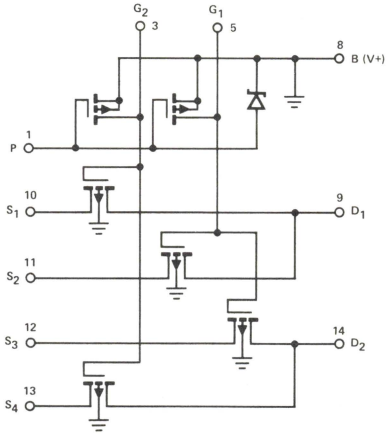
DESCRIPTION

The G122 contains four enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated onto a silicon substrate (body) and are internally connected into two groups of two switches per group. This arrangement facilitates the switching or multiplexing of differential analog signals. Each group has a common drain terminal (D_1 and D_2) which will function equally well as a common source. Each gate terminal (G) controls a pair of switches and is provided with a normally-OFF "pull-up" MOS FET which may be turned ON to provide a current source to a gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

FUNCTIONAL DIAGRAM

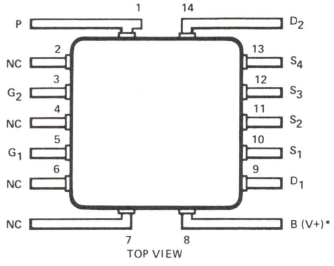


SCHEMATIC DIAGRAM



PIN CONFIGURATION

Flat Package



ORDER NUMBER: G122AL
SEE PACKAGE 5

*Common to Substrate and Base of Package

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ABSOLUTE MAXIMUM RATINGS

V_B to V_S	−2 to 30 V
V_B to V_D	−2 to 30 V
V_D to V_S	±30 V
V_B to V_G or V_P	35 V
I_S, I_D	100 mA
I_G	5 mA
I_P	100 μA

Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	750 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 75°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	MAX LIMITS A SUFFIX 25°C	MAX LIMITS A SUFFIX 125°C	MAX LIMITS B SUFFIX −20°C	MAX LIMITS B SUFFIX 25°C	MAX LIMITS B SUFFIX 85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0	
1		$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V	I_S = −1 mA
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V	
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current		0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0	
5		$I_{D(off)}$	Drain OFF Leakage Current		−1	−1000		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0	
6	STATIC	$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V	
7		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V	
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{GD} = 0, V_{SB} = 0	
9		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −10 μA, V_{GS} = 0, V_{SB} = 0	
10		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0	
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_S = −10 μA	
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0	
13		C_{gs}	Gate-Source Capacitance		1.8 Typ*			1.8 Typ*		pF	V_{DB} = V_{SB} = 0 Body Guarded	Drain Guarded
14	DYNAMIC	C_{gd}	Gate-Drain Capacitance		1.8 Typ*			1.8 Typ*				Source Guarded
15		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded
16		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded
17		C_{db}	Drain-Body Capacitance		6 Typ*			6 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded

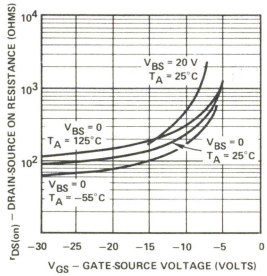
V_{GB} = 0, f = 1 MHz

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

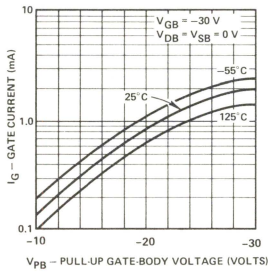
MABB

TYPICAL CHARACTERISTICS

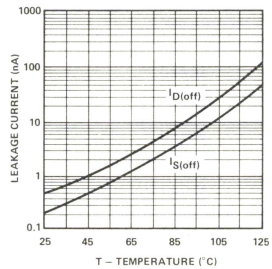
$r_{DS(on)}$ vs V_{GS} and Temperature



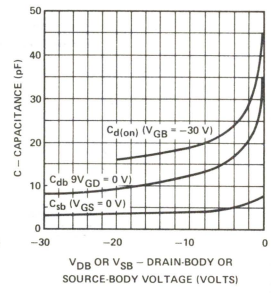
I_G vs V_{PB}



$I_{S(off)}$ vs Temperature



Capacitance vs V_{DB} and V_{GS}



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Monolithic 4-Channel Enhancement-Type MOS FET Switch

Siliconix

designed for . . .

- **Switching Analog Signals**
- **Multiplexing**

BENEFITS

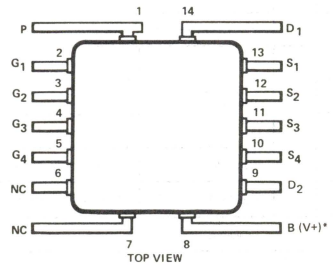
- **Reduces External Component Requirements**
  - Internal Zener Diode Protects the Gate
  - Four Switches Per Chip
  - Intergrated MOS FET for Each Gate to Provide "Pull-Up" Current for Gate-Driver Circuit

DESCRIPTION

The G123 contains four enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The switches are integrated on a silicon substrate (body). Separate source and gate connections are provided for each switch; the drains are connected in pairs to two drain terminals. Functions of the drain and source terminals may be interchanged with comparable performance. Each gate terminal (G) is provided with a normally-OFF "pull-up" MOS FET which may be turned ON to provide a current source to a gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

PIN CONFIGURATIONS

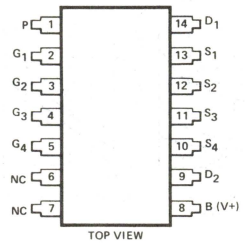
Flat Package



ORDER NUMBER: G123AL
SEE PACKAGE 5

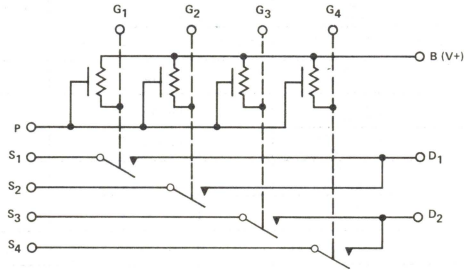
*Common to Substrate and Base of Package

Dual-In-Line Package

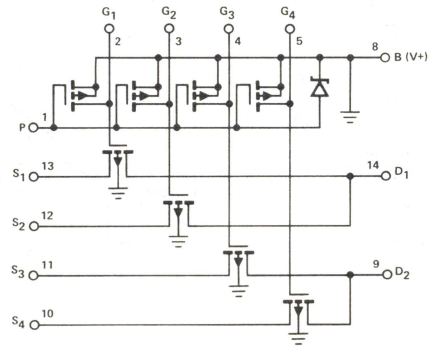


ORDER NUMBERS: G123AP OR G123BP
SEE PACKAGE 11

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

V_B to V_S	−2 to 35 V
V_B to V_D	−2 to 30 V
V_D to V_S	±30 V
V_B to V_G or V_P	35 V
I_S, I_D	100 mA
I_G	5 mA
I_P	100 μA
Storage Temperature	−65 to 150°C
Operating Temperature (A Suffix)	−55 to 125°C
(B Suffix)	−20 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14 Pin DIP***	825 mW

*All leads soldered or welded or PC board.

**Derate 10 mW/°C above 75°C.

***Derate 11 mW/°C above 75°C

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

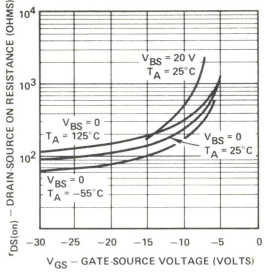
		CHARACTERISTIC		MAX LIMITS A SUFFIX −55°C	25°C	125°C	MAX LIMITS B SUFFIX −20°C	25°C	85°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V_{DB} = 0, V_{PB} = 0		
1		$r_{DS(on)}$	Drain-Source ON Resistance	100	100	125	125	125	150	Ω	V_{DB} = 0, V_{GD} = −30 V		
2				200	200	250	250	250	300		V_{DB} = −10 V, V_{GD} = −20 V	I_S = −1 mA	
3				450	450	600	500	500	600		V_{DB} = −20 V, V_{GD} = −10 V		
4		$I_{S(off)}$	Source OFF Leakage Current		−0.5	−500		−5	−500	nA	V_{SD} = −20 V, V_{GD} = 0		
5		$I_{D(off)}$	Drain OFF Leakage Current		−1	−1000		−10	−1000		V_{DS} = −20 V, V_{GS} = 0, V_{SB} = 0		
6	STATIC	$I_{G(on)}$	Gate ON Current		−0.8 to −2.4			−0.8 to −2.4		mA	V_{GB} = −30 V, V_{PB} = −30 V		
7		I_{GSS}	Gate-Channel Leakage Current		−0.5	−500		−5	−500	nA	V_{GB} = −20 V		
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	−1.5 to −4.0	V	I_D = −10 μA, V_{GD} = 0, V_{SB} = 0		
9		BV_{DSS} Min	Drain-Source Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_D = −10 μA, V_{GS} = 0, V_{SB} = 0		
10		BV_{SDS} Min	Source-Drain Breakdown Voltage	−30	−30	−30	−30	−30	−30		I_S = −10 μA, V_{GD} = 0		
11		BV_{GBS} Min	Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_G = −10 μA		
12		BV_{PBS} Min	Pull-Up Gate-Body Breakdown Voltage	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90	−35 to −90		I_P = −10 μA, V_{GB} = 0		
13	DYNAMIC	C_{gs}	Gate-Source Capacitance		1.8 Typ*			1.8 Typ*		pF	V_{DB} = V_{SB} = 0 Body Guarded	Drain Guarded	V_{GB} = 0 f = 1 MHz
14		C_{gd}	Gate-Drain Capacitance		1.8 Typ*			1.8 Typ*				Source Guarded	
15		$C_{ds(off)}$	Drain-Source OFF Capacitance		0.4 Typ*			0.4 Typ*				Gate Guarded	
16		C_{sb}	Source-Body Capacitance		2 Typ*			2 Typ*			V_{DB} = 0, V_{SB} = −5 V	Gate and Drain Guarded	
17		C_{db}	Drain-Body Capacitance		6 Typ*			6 Typ*			V_{SB} = 0, V_{DB} = −5 V	Gate and Source Guarded	

*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

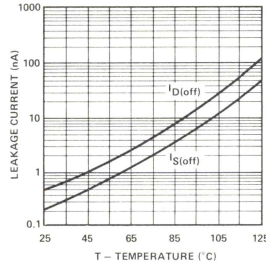
MAB-C

TYPICAL CHARACTERISTICS

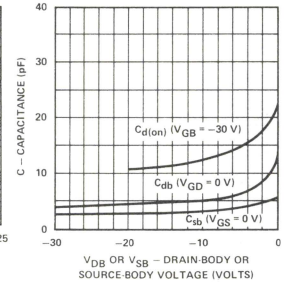
$r_{DS(on)}$ vs V_{GS} and Temperature



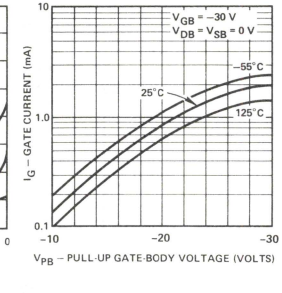
$I_{S(off)}$ vs Temperature



Capacitance vs V_{DB} and V_{GS}



I_G vs V_{PB}



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DIE TOPOGRAPHY INDEX

Device Number	Technology	Page No.
DGM111	PMOS Switches	4-4
DGM122		4-4
DG123		4-4
DG125		4-5
DG126, DG134	JFET Switches	4-5, 4-6
DG129, DG133		4-5, 4-6
DG139, DG144		4-6, 4-7
DG140, DG141		4-5, 4-6
DG142, DG143		4-6, 4-7
DG145, DG146		4-6, 4-7
DG151, DG153		4-6, 4-5
DG152, DG154		4-6 4-5
DG161, DG163		4-7, 4-6
DG162, DG164		4-7, 4-6
DG170	PMOS Switches	4-7
DG172		4-8
DG173		4-8
DG180	JFET Switches	4-8
DG181		4-8
DG182		4-8
DG183		4-9
DG184		4-9
DG185		4-9
DG186		4-9
DG187		4-9
DG188		4-9
DG189		4-10
DG190		4-10
DG191		4-10
DG200	CMOS Switches	4-10
DG201		4-11
DG281	JFET Switches	4-8
DG284		4-9
DG287		4-9
DG290		4-10

Device Number	Technology	Page No.
DG300	CMOS Switches	4-11
DG301		4-12
DG302		4-13
DG303		4-13
DG304		4-11
DG305		4-12
DG306		4-14
DG307		4-14
DG381		4-14
DG384		4-15
DG387		4-15
DG390		4-15
DG501	PMOS Multiplexers	4-16
DG503		4-16
DG506	CMOS Multiplexers	4-17
DG507		4-18
DG508		4-19
DG509		4-19
DG515		4-20
DG516		4-20
Si3002	PMOS Switches	4-20
Si3705		4-21
D123	Bipolar Drivers	4-21
D125		4-21
D129		4-22
D139		4-22
G115	PMOS FETs	4-23
G116		4-23
G117		4-23
G118		4-23
G119		4-24
G122		4-24
G123		4-24
G124		4-23

Analog Switches 1
Drivers for FET Switches 2
Multi-Channel FETs 3
Die Process and Topography Information 4
Burn-In Pin Connections 5
Mechanical Data 6
Appendices 7

Die Process Information

Siliconix is a large-volume supplier of die to the hybrid industry. Both military and industrial grades are available. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

Physical Data

Physical layout and dimensions are presented in the Die Topography section. Die are supplied to length and width dimensions which have an accuracy of ±.003 inches.

Bonding pad location may be identified from the die topography shown. Contact factory for ordering information.

Each die or wafer is passivated with approximately 8,000 angstroms of non-crystalline glass.

Die are supplied without gold backing. Gold backing is available as an option.

Die metallization is deposited aluminum approximately 12,000 angstroms thick.

Die Screening Criteria

Electrical Probe – All dice are 100% probed in wafer form at 25°C to DC criteria designed to support "A" Suffix data sheet limits. An optional screen to "C" Suffix limits is available.

Visual Criteria – Each die receives a visual inspection to MIL-STD-883 Method 2010 Condition B criteria. Siliconix QC Department samples each lot to an LTPD of 10%.

Alternate visual criteria, including Method 2010 Condition A or Siliconix Industrial criteria, are available.

Packaging

Die are supplied in dust-proof, anti-static waffle packs (see illustration).

Assembly

Die supplied in waffle packs normally do not need cleaning, while wafers need to be cleaned. The ink currently used is soluble in most alcohols.

Die may be handled either with a "protected tip" vacuum pick-up or with die attach tweezers.

Die attach may be gold eutectic or conductive epoxy.

Die bonding pads are aluminum and may be lead bonded using either thermal compression gold wire or ultrasonically bonded aluminum wire.

The customer's interests will best be served if static sensitivity handling procedures are used.

Part Number Designations

Dice supplied to "A" Suffix testing limits, Condition B (MIL-STD-883), visual and waffle packed, have a part number suffix designation of "ADICE".

Example: The DG200AA supplied in die form would be **DG200ADICE**. (See die ordering information.)

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Die Process Information (Continued)

Options

(Price will be quoted upon request.)

SEM – Scanning electron microscope examination and control in accordance with MIL-STD-883 Method 2018 can be ordered on die and wafers.

Wafer Qualification to Unprobed Parameters

Wafer Qualification to Unprobed Parameters – Sample testing of purchased die to demonstrate capability to perform at data sheet temperature extremes or to switching time test limits by use of LTPD techniques can be provided.

Alternate Visual Criteria – Siliconix offers visual inspection to internal Siliconix specification 5018 as an alternative for the Industrial/Commercial user, at a reduced price. ("IDICE" ordering information.)

Visual inspection to customer generated specifications can be provided.

Alternate Electrical Probe – A 100% DC electrical probe to support "C" Suffix 25°C electrical specs is available. ("IDICE" ordering information.)

Gold Backing – Die may be purchased with gold alloyed to the backside. This is a special order item. Gold thickness would be as follows:

- FETs (NC, NIP) –750Å min
- IC's (all) –4500Å min

Hot Probe – Siliconix has a chip processor/distribution with hot probe capability available.

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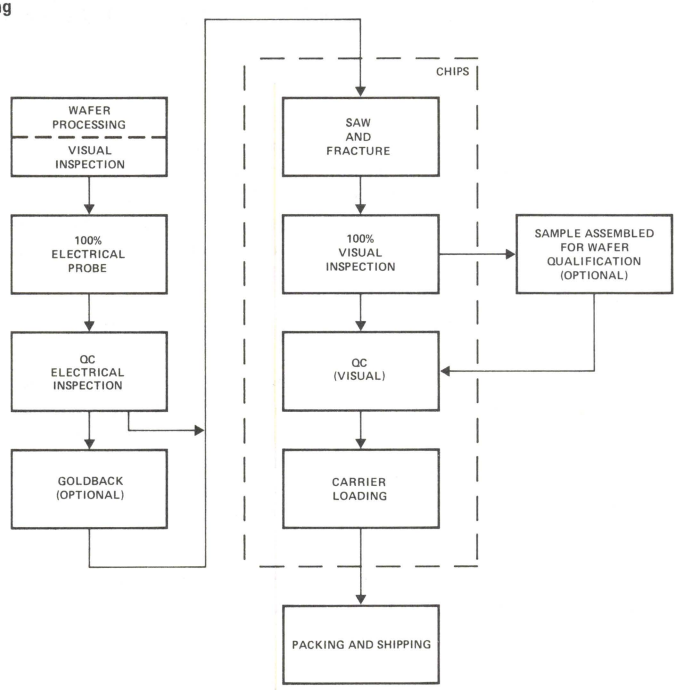
Die Process Information (Continued)

Chip and Wafer Processing



Chip Packaging

Chips are packaged as individual die in the flat waffle carrier illustrated in Figure 1. The carrier has a cavity size adequate to allow ease of loading/unloading and also prevents die from rotating within the cavity.

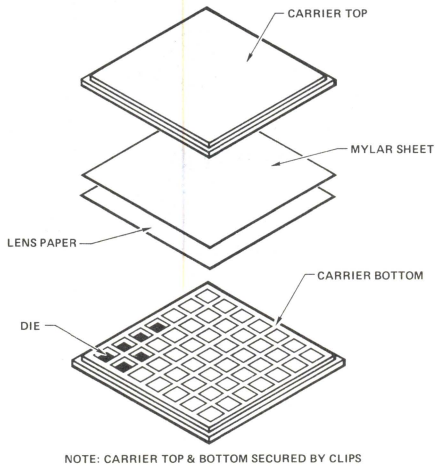


Figure 1

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Siliconix

Die Topography Information

Some of Siliconix's analog switches are of multi-chip design with inter-chip connections. The DG123, for example, consists of a separate driver chip (EID) and a separate MOS switch chip (MABA). Figure 1 illustrates the bonding arrangement in the DIP package. Note that the two chips are mounted on electrically separate islands. This is due to the different substrate potentials, the MABA substrate is at the positive supply voltage while the EID substrate is at the negative supply voltage.

The JFET switches, for example, are also of multi-chip design. The DG190 consists of a separate driver chip (CMJB) and four separate JFET transistors (NC). Figure 2 illustrates the bonding diagram arrangement in the DIP package. The driver and the JFET switches are mounted so that the substrates are electrically isolated. The substrate of the driver is at the negative supply voltage while the substrate of the JFET switches is the gate connection. A bond wire connects the driver to the JFET gate.

The pin connections for the JFET switch chips can be determined from the chip section and switch pin-out in the data sheet. For example, from the DG190 pin configuration we see that the DG190 has 4 JFETs in one package; D_3 and S_3 are the drain and source of the third JFET.

Die Diagrams/Dimensions

These negative image photos are of the metallization pattern. Scale is ≈32x. Bonding pads are 4 mil (0.10 mm) square, glass-free aluminum metallization. Pad identification numbers correspond to pin numbers for the dual-in-line package on data sheets. The "geometry" is an alpha code used in the factory for identification.

The following pages contain layout, die dimensions and pad identification.

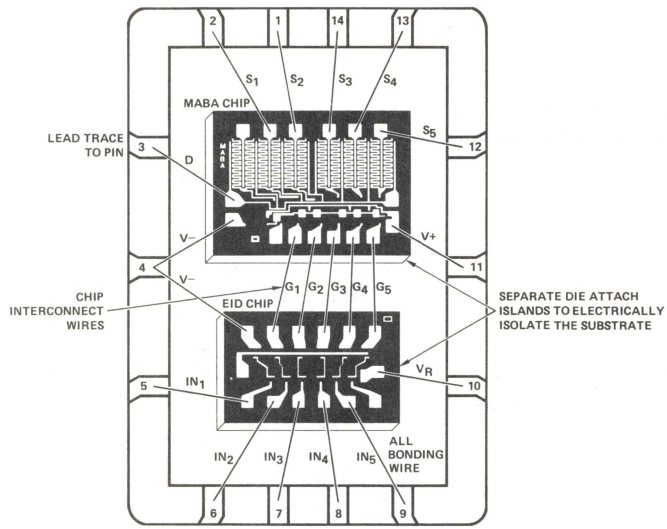

Figure 1. DG123 Analog Switch (Multi-Chip)

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Siliconix

Die Topography Information (Continued)

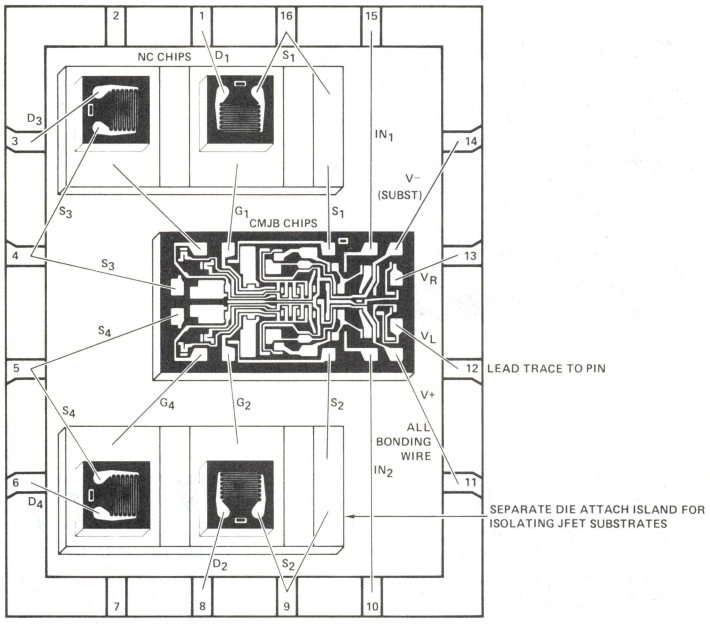

Figure 2. DG190 JFET Analog Switch

NOTE: Die Topography is *for reference only*

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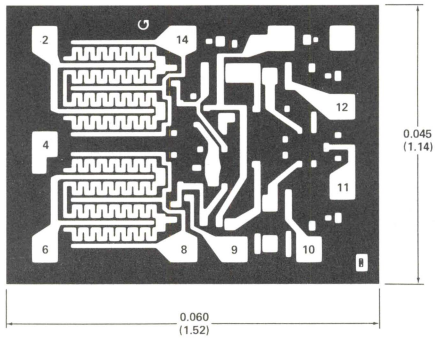
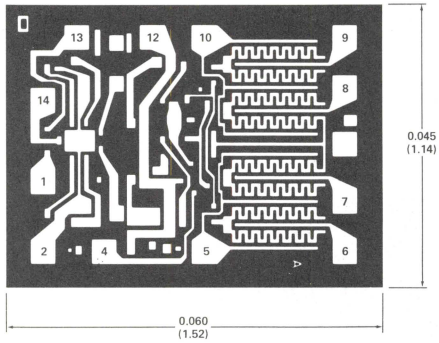


PIN NO.	FUNCTION
2	DRAIN 1
4	V– (SUBSTRATE)
6	DRAIN 2
8	SOURCE 2
9	V+
10	LOGIC INPUT 2
11	V_L
12	LOGIC INPUT 1
14	SOURCE 1

Pin numbers are for dual in-line packages

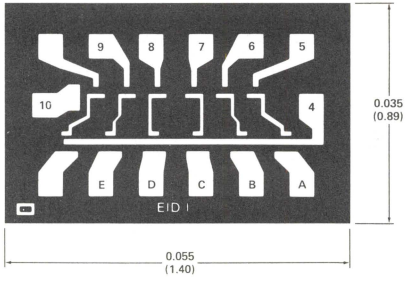
DGM111



PIN NO.	FUNCTION
1	INPUT 2
2	V_R
4	V+
5	DRAIN 1
6	SOURCE 1
7	SOURCE 2
8	SOURCE 4
9	SOURCE 3
10	DRAIN 2
12	V– (SUBSTRATE)
13	INPUT 1
14	V_L

Pin numbers are for dual in-line packages

DGM122

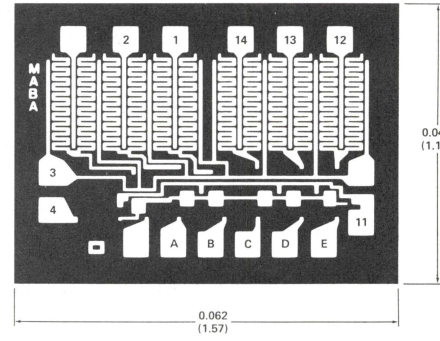


PIN NO.	FUNCTION
4	V– (SUBSTRATE)
5	INPUT 1
6	INPUT 2
7	INPUT 3
8	INPUT 4
9	INPUT 5
10	V_R

INTERCHIP PAD CONNECTIONS	
A	TO GATE 1
B	TO GATE 2
C	TO GATE 3
D	TO GATE 4
E	TO GATE 5

DG123
DRIVER CHIP

Pin numbers are for dual in-line packages



PIN NO.	FUNCTION
1	SOURCE 2
2	SOURCE 1
3	DRAIN
4	V–
11	V+ (SUBSTRATE)
12	SOURCE 5
13	SOURCE 4
14	SOURCE 3

INTERCHIP PAD CONNECTIONS	
A	GATE 1
B	GATE 2
C	GATE 3
D	GATE 4
E	GATE 5

MOS SWITCH CHIP

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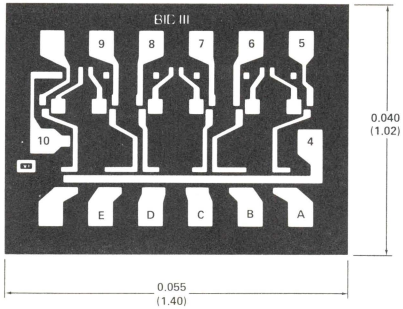
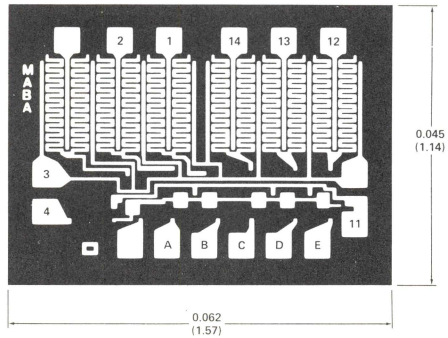


PIN NO.	FUNCTION
4	V– (SUBSTRATE)
5	INPUT 1
6	INPUT 2
7	INPUT 3
8	INPUT 4
9	INPUT 5
10	V_L

INTERCHIP PAD CONNECTIONS	
A	TO GATE 1
B	TO GATE 2
C	TO GATE 3
D	TO GATE 4
E	TO GATE 5

DG125
DRIVER CHIP

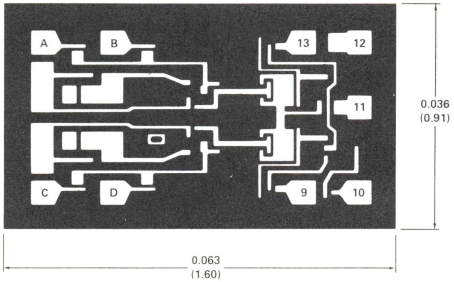
Pin numbers are for dual in-line packages



PIN NO.	FUNCTION
1	SOURCE 2
2	SOURCE 1
3	DRAIN
4	V–
11	V+ (SUBSTRATE)
12	SOURCE 5
13	SOURCE 4
14	SOURCE 3

INTERCHIP PAD CONNECTIONS	
A	GATE 1
B	GATE 2
C	GATE 3
D	GATE 4
E	GATE 5

MOS SWITCH CHIP

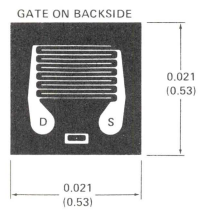


PIN NO.	FUNCTION
9	INPUT 1
10	V_R
11	V+
12	V– (SUBSTRATE)
13	INPUT 2

Pin numbers are for dual in-line packages

DRIVER CHIP

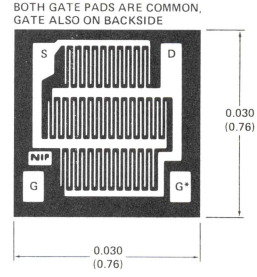
INTERCHIP CONNECTIONS	
A	TO GATE 4
B	TO GATE 2
C	TO GATE 3
D	TO GATE 1



INTERCHIP CONNECTIONS	FUNCTION
D	DRAIN
S	SOURCE

Gate is on backside of chip

30, 75 Ω
JFET SWITCH CHIP



INTERCHIP CONNECTIONS	FUNCTION
D	DRAIN
S	SOURCE
G	GATE

* Either gate pad may be used, gate connection is also on backside of chip

10 Ω
JFET SWITCH CHIP

DEVICE	JFET USED	NO. OF JFETs
DG126	75 Ω	4
DG129	30 Ω	4
DG140	10 Ω	4
DG153	10 Ω	4
DG154	30 Ω	4

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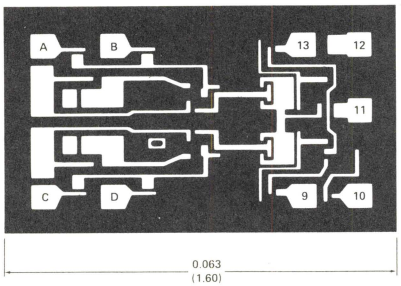
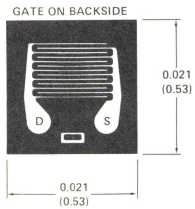
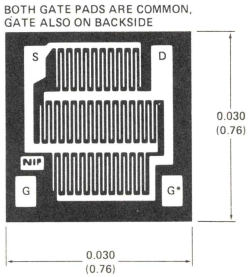






PIN NO.	FUNCTION
9	INPUT 1
10	V_R
11	V+
12	V– (SUBSTRATE)
13	INPUT 2

Pin numbers are for dual in-line packages

INTERCHIP CONNECTIONS	
A	TO GATE 2
B	NO CONNECTION
C	TO GATE 1
D	NO CONNECTION

DRIVER CHIP

INTERCHIP CONNECTIONS	FUNCTION
D	DRAIN
S	SOURCE

Gate is on backside of chip

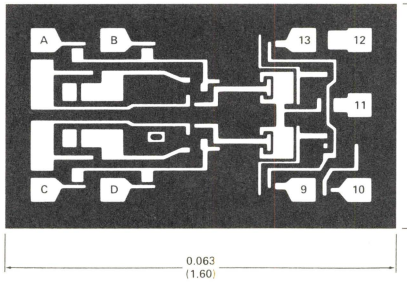
30, 75 Ω
JFET SWITCH CHIP

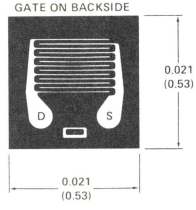
INTERCHIP CONNECTIONS	FUNCTION
D	DRAIN
S	SOURCE
G	GATE

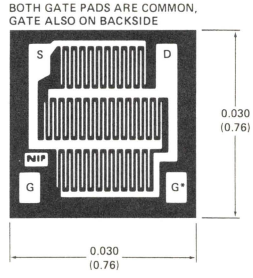
*Either gate pad may be used, gate connection is also on backside of chip

10 Ω
JFET SWITCH CHIP

DEVICE	JFET USED	NO. OF JFETs
DG133	30 Ω	2
DG134	75 Ω	2
DG141	10 Ω	2
DG151	10 Ω	2
DG152	30 Ω	2







PIN NO.	FUNCTION
9	INPUT 1
10	V_R
11	V+
12	V– (SUBSTRATE)
13	INPUT 2

Pin numbers are for dual in-line packages

INTERCHIP CONNECTIONS	
A	TO GATE 4
B	TO GATE 2
C	TO GATE 3
D	TO GATE 1

DRIVER CHIP

INTERCHIP CONNECTIONS	FUNCTION
D	DRAIN
S	SOURCE

Gate is on backside of chip

30, 75 Ω
JFET SWITCH CHIP

INTERCHIP CONNECTIONS	FUNCTION
D	DRAIN
S	SOURCE
G	GATE

*Either gate pad may be used, gate connection is also on backside of chip

10 Ω
JFET SWITCH CHIP

DEVICE	JFET USED	NO. ON JFETs
DG139	30 Ω	4
DG142	75 Ω	4
DG145	10 Ω	4
DG163	10 Ω	4
DG164	30 Ω	4

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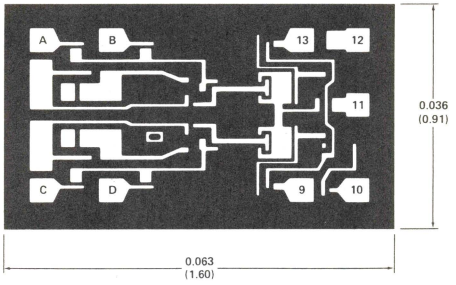
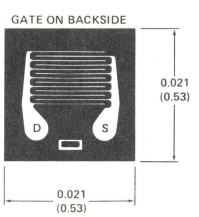


PIN NO.	FUNCTION
9	INPUT 1
10	V_R
11	V+
12	V– (SUBSTRATE)
13	INPUT 2

Pin numbers are for dual in-line packages

INTERCHIP CONNECTIONS	
A	TO GATE 2
B	NO CONNECTION
C	TO GATE 1
D	NO CONNECTION

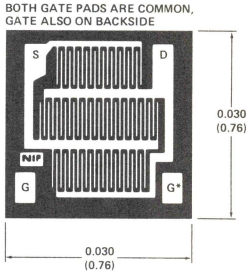
DRIVER CHIP



INTERCHIP CONNECTIONS	FUNCTION
D	DRAIN
S	SOURCE

Gate is on backside of chip

30, 75 Ω JFET SWITCH CHIP

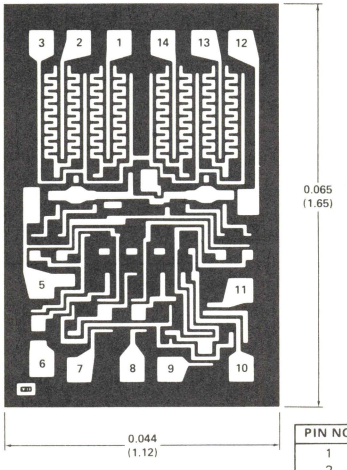


INTERCHIP CONNECTIONS	FUNCTION
D	DRAIN
S	SOURCE
G	GATE

*Either gate pad may be used, gate connection is also on backside of chip

10 Ω JFET SWITCH CHIP

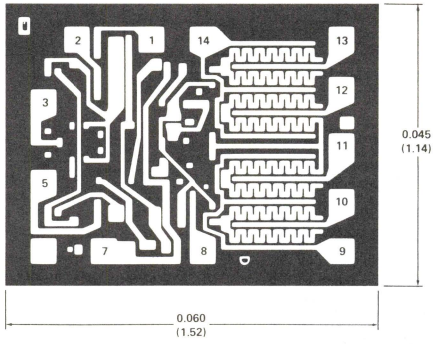
DEVICE	JFET USED	NO. OF JFETs
DG143	75 Ω	2
DG144	30 Ω	2
DG146	10 Ω	2
DG161	10 Ω	2
DG162	30 Ω	2



Pin numbers are for dual in-line packages

PIN NO.	FUNCTION
1	SOURCE 3
2	SOURCE 4
3	DRAIN
5	V– (SUBSTRATE)
6	INPUT 4
7	INPUT 3
8	INPUT 2
9	INPUT 1
10	V_L
11	V_R
12	V+
13	SOURCE 1
14	SOURCE 2

DG172



PIN NO.	FUNCTION
1	INPUT 1
2	INPUT 2
3	V_L
5	V_R
7	V– (SUBSTRATE)
8	V+
9	DRAIN 2
10	SOURCE 4
11	SOURCE 3
12	SOURCE 1
13	SOURCE 2
14	DRAIN 1

Pin numbers are for dual in-line packages

DG173

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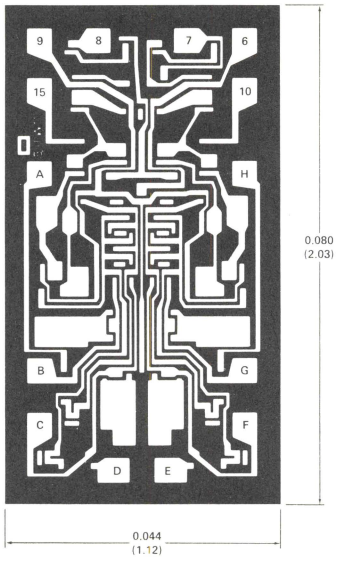


DRIVER CHIP

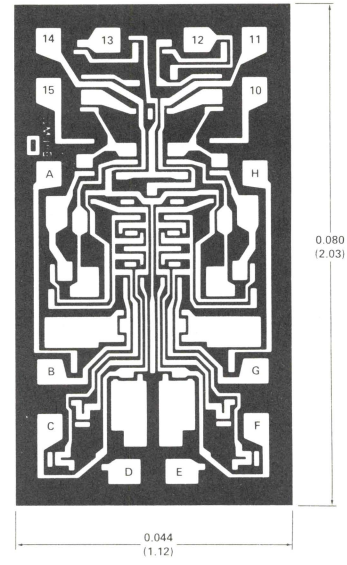
DEVICE	JFET USED	NO. OF JFETs
DG180	10 Ω	2
DG181	30 Ω	2
DG182	75 Ω	2
DG281	300 Ω	2

PIN NO.	FUNCTION
6	V+
7	V_L
8	V_R
9	V− (SUBSTRATE)
10	INPUT 2
15	INPUT 1

Pin numbers are for dual in-line packages

INTERCHIP PAD CONNECTIONS	
A	NO CONNECTION
B	NO CONNECTION
C	TO JFET 2, GATE
D	FROM JFET 2, SOURCE
E	FROM JFET 1, SOURCE
F	TO JFET 1, GATE
G	NO CONNECTION
H	NO CONNECTION

Substrate is V−



DRIVER CHIP

DEVICE	JFET USED	NO. OF JFETs
DG183	10 Ω	4
DG184	30 Ω	4
DG185	75 Ω	4
DG284	300 Ω	4

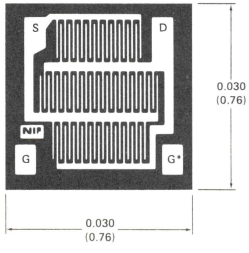
PIN NO.	FUNCTION
10	INPUT 2
11	V+
12	V_L
13	V_R
14	V− (SUBSTRATE)
15	INPUT 1

Pin numbers are for dual in-line packages.

INTERCHIP PAD CONNECTIONS	
A	FROM JFET 1, SOURCE
B	TO JFET 1, GATE
C	TO JFET 3, GATE
D	FROM JFET 3, SOURCE
E	FROM JFET 4, SOURCE
F	TO JFET 4, GATE
G	TO JFET 2, GATE
H	FROM JFET 2, SOURCE

Substrate is V−

BOTH GATE PADS ARE COMMON, GATE ALSO ON BACKSIDE

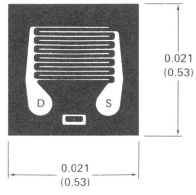


INTERCHIP PAD CONNECTIONS	FUNCTION
S	SOURCE
D	DRAIN
G	GATE

*Either gate pad can be used, backside is also gate

10 Ω JFET SWITCH CHIP

GATE ON BACKSIDE

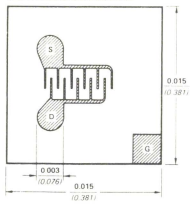


INTERCHIP PAD CONNECTIONS	FUNCTION
S	SOURCE
D	DRAIN

Gate is backside contact

30, 75 Ω JFET SWITCH CHIP

GATE ALSO BACKSIDE CONTACT



INTERCHIP PAD CONNECTIONS	FUNCTION
S	SOURCE
D	DRAIN
G	GATE

300 Ω JFET SWITCH CHIP

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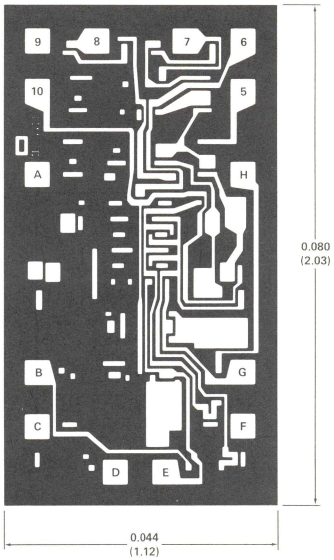


DRIVER CHIP

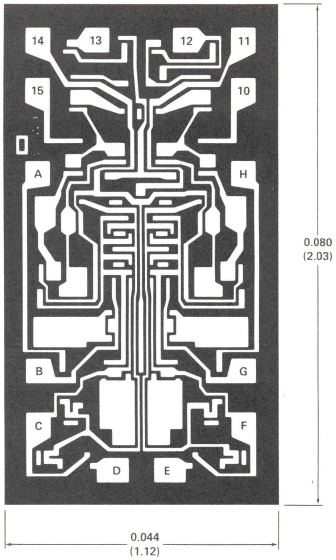
DEVICE	JFET USED	NO. OF JFETs
DG186	10 Ω	2
DG187	30 Ω	2
DG188	75 Ω	2
DG287	300 Ω	2

PIN NO.	FUNCTION
5	INPUT 1
6	V+
7	V_L
8	V_R
9	NOT CONNECTED
10	V− (SUBSTRATE)

INTERCHIP PAD CONNECTIONS	
A	NOT CONNECTED
B	FROM JFET 2, SOURCE
C	NOT CONNECTED
D	NOT CONNECTED
E	TO JFET 2, GATE
F	NOT CONNECTED
G	TO JFET 1, GATE
H	FROM JFET 1, SOURCE

Pin numbers are for dual in-line packages

Substrate is V−



DRIVER CHIP

DEVICE	JFET USED	NO. OF JFETs
DG189	10 Ω	4
DG190	30 Ω	4
DG191	75 Ω	4
DG290	300 Ω	4

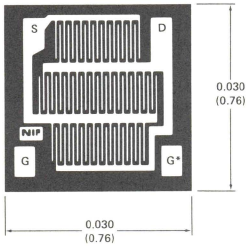
PIN NO.	FUNCTION
10	INPUT 2
11	V+
12	V_L
13	V_R
14	V− (SUBSTRATE)
15	INPUT 1

INTERCHIP PAD CONNECTIONS	
A	FROM JFET 1, SOURCE
B	TO JFET 1, GATE
C	TO JFET 3, GATE
D	FROM JFET 3, SOURCE
E	FROM JFET 4, SOURCE
F	TO JFET 4, GATE
G	TO JFET 2, GATE
H	FROM JFET 2, SOURCE

Pin numbers are for dual in-line packages

Substrate is V−

BOTH GATE PADS ARE COMMON, GATE ALSO ON BACKSIDE

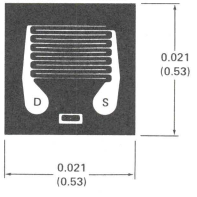


INTERCHIP PAD CONNECTIONS	FUNCTION
S	SOURCE
D	DRAIN
G	GATE

* Either gate pad can be used, backside is also gate

10 Ω JFET SWITCH CHIP

GATE ON BACKSIDE

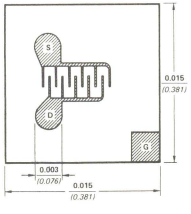


INTERCHIP PAD CONNECTIONS	FUNCTION
S	SOURCE
D	DRAIN

Gate is backside contact

30, 75 Ω JFET SWITCH CHIP

GATE ALSO BACKSIDE CONTACT



INTERCHIP PAD CONNECTIONS	FUNCTION
S	SOURCE
D	DRAIN
G	GATE

300 Ω JFET SWITCH CHIP

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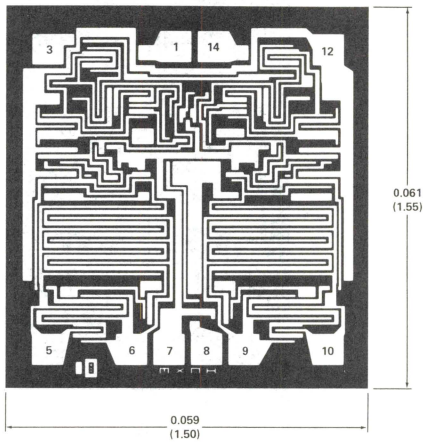
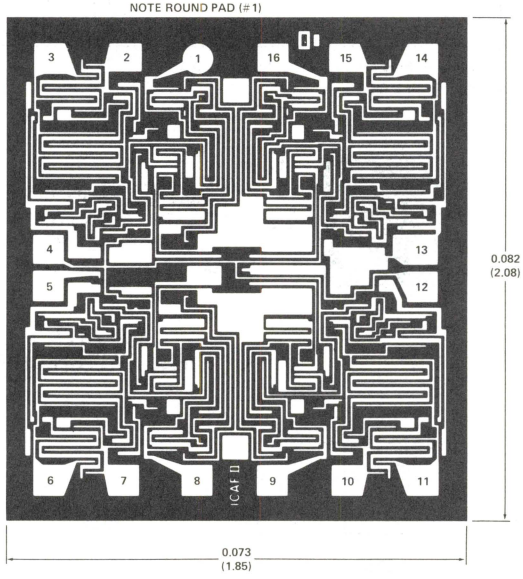


PIN NO.	FUNCTION
1	INPUT 2
3	GROUND
5	SOURCE 2
6	DRAIN 2
7	V–
8	V_{REF}
9	DRAIN 1
10	SOURCE 1
12	V+ (SUBSTRATE)
14	INPUT 1

Pin numbers are for dual in line packages

DG200



PIN NO.	FUNCTION
1	INPUT 1
2	DRAIN 1
3	SOURCE 1
4	V–
5	GND
6	SOURCE 4
7	DRAIN 4
8	INPUT 4
9	INPUT 3
10	DRAIN 3
11	SOURCE 3
12	V_{REF}
13	V+ (SUBSTRATE)
14	SOURCE 2
15	DRAIN 2
16	INPUT 2

Pin numbers are for dual in line packages

DG201

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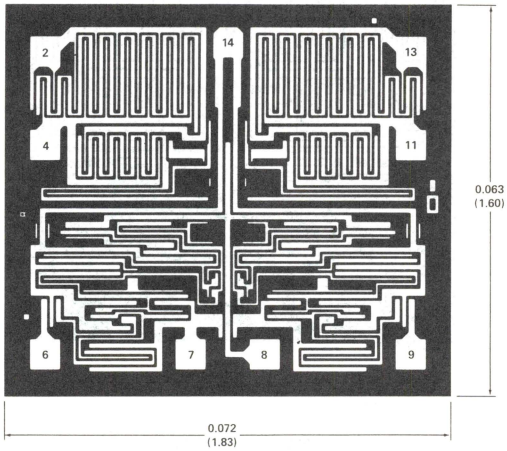
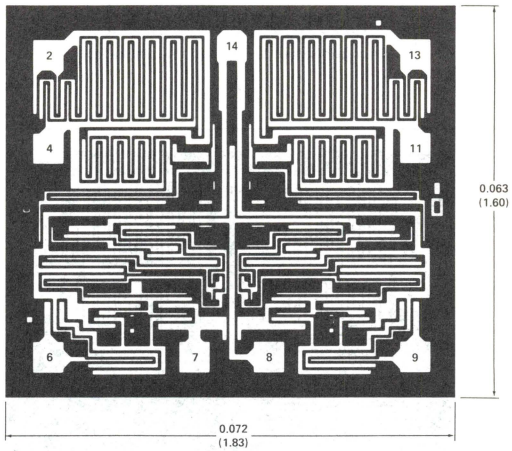


DG300



DG304

PIN NO.	FUNCTION
2	DRAIN 1
4	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
9	INPUT 2
11	SOURCE 2
13	DRAIN 2
14	V+ (SUBSTRATE)

Pin numbers are for dual in-line packages

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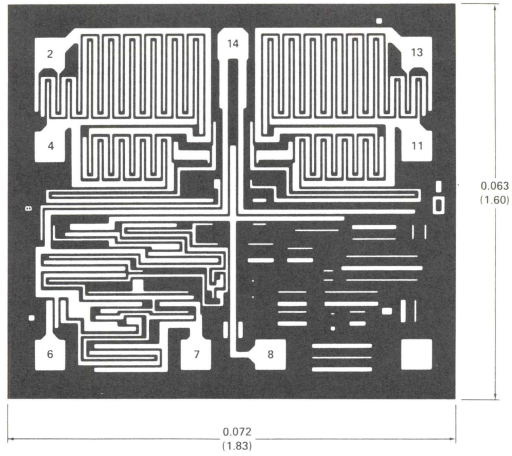
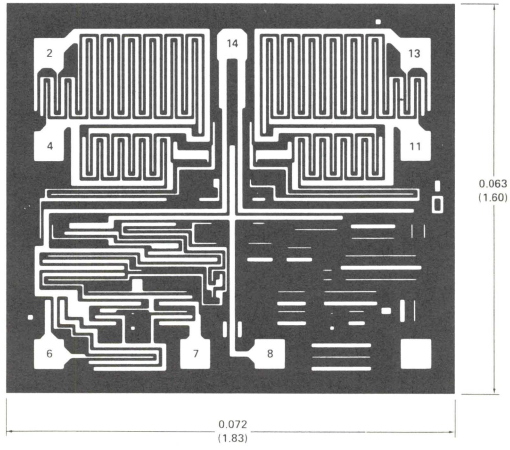


PIN NO.	FUNCTION
2	DRAIN 1
4	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
11	SOURCE 2
13	DRAIN 2
14	V+ (SUBSTRATE)

Pin numbers are for dual in-line packages

DG301



PIN NO.	FUNCTION
2	DRAIN 1
4	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
11	SOURCE 2
13	DRAIN 2
14	V+ (SUBSTRATE)

Pin numbers for dual in-line packages

DG305

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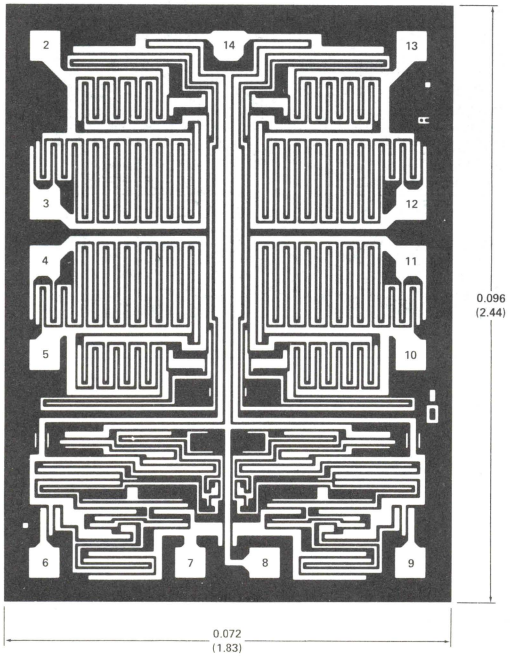

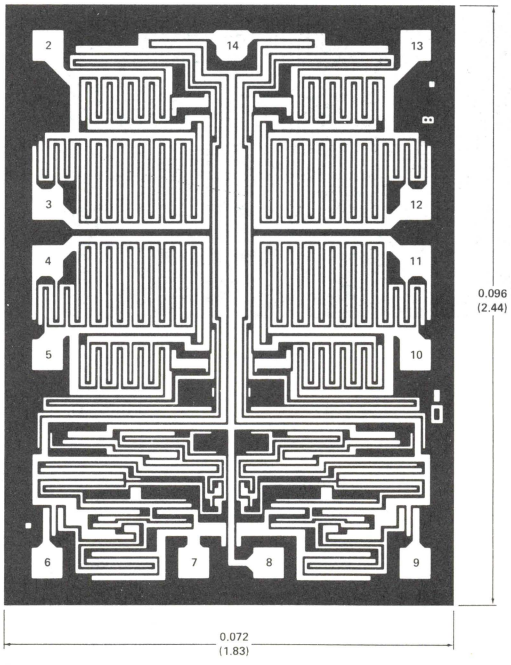

PIN NO.	FUNCTION
2	SOURCE 3
3	DRAIN 3
4	DRAIN 1
5	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
9	INPUT 2
10	SOURCE 2
11	DRAIN 2
12	DRAIN 4
13	SOURCE 4
14	V+ (SUBSTRATE)

Pin numbers are for dual in-line packages

DG302

DG303

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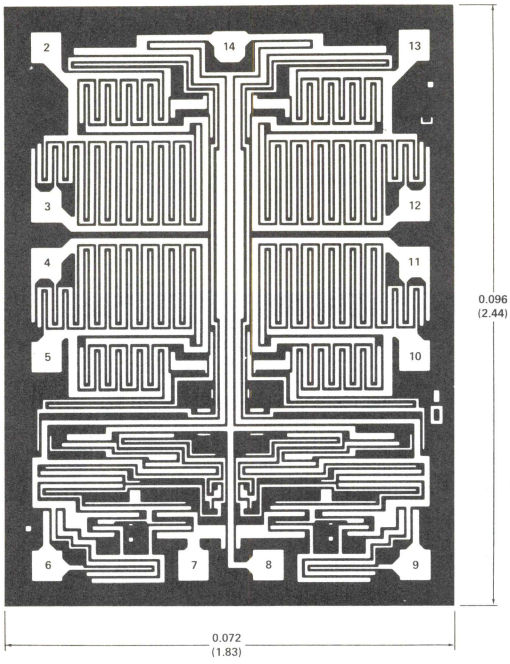
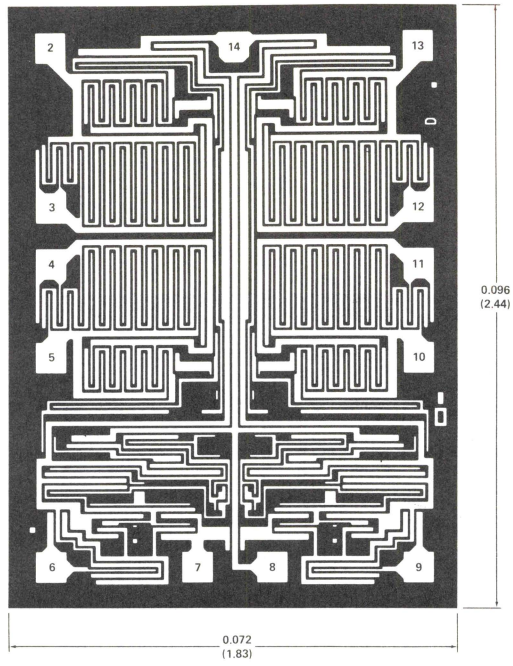


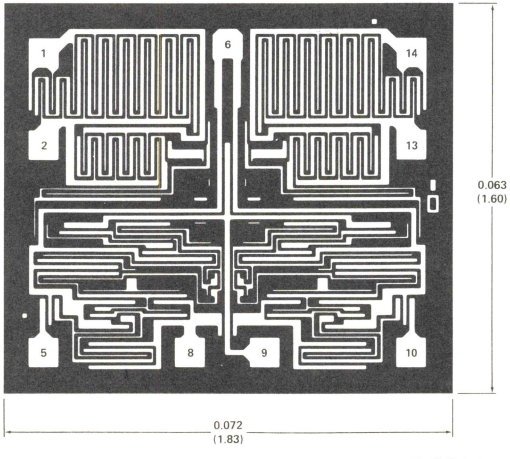


PIN NO.	FUNCTION
2	SOURCE 3
3	DRAIN 3
4	DRAIN 1
5	SOURCE 1
6	INPUT 1
7	GROUND
8	V–
9	INPUT 2
10	SOURCE 2
11	DRAIN 2
12	DRAIN 4
13	SOURCE 4
14	V+ (SUBSTRATE)

DG306

Pin numbers are for dual in-line packages

DG307



PIN NO.	FUNCTION
1	SOURCE 1
2	DRAIN 1
5	INPUT 1
6	V+ (SUBSTRATE)
8	V_R
9	V–
10	INPUT 2
13	DRAIN 2
14	SOURCE 2

Pin numbers are for dual in-line packages

DG381

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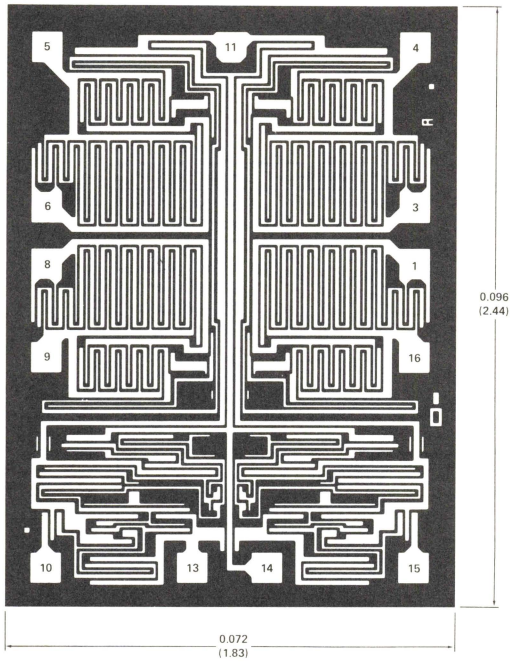
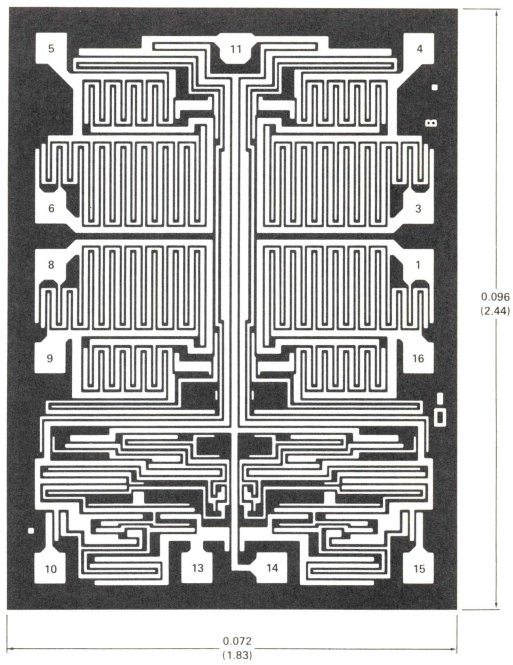


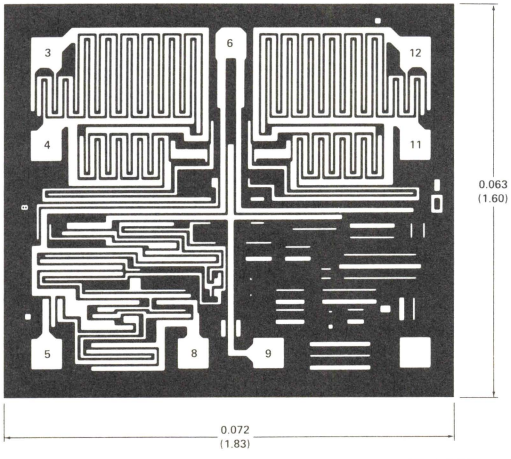


PIN NO.	FUNCTION
1	DRAIN 1
3	DRAIN 3
4	SOURCE 3
5	SOURCE 4
6	DRAIN 4
8	DRAIN 2
9	SOURCE 2
10	INPUT 2
11	V+ (SUBSTRATE)
13	GROUND
14	V–
15	INPUT 1
16	SOURCE 1

DG384

Pin numbers are for dual in-line packages

DG390



PIN NO.	FUNCTION
3	DRAIN 1
4	SOURCE 1
5	INPUT 1
6	V+ (SUBSTRATE)
8	V_R
9	V–
11	SOURCE 2
12	DRAIN 2

Pin numbers are for dual in-line packages

DG387

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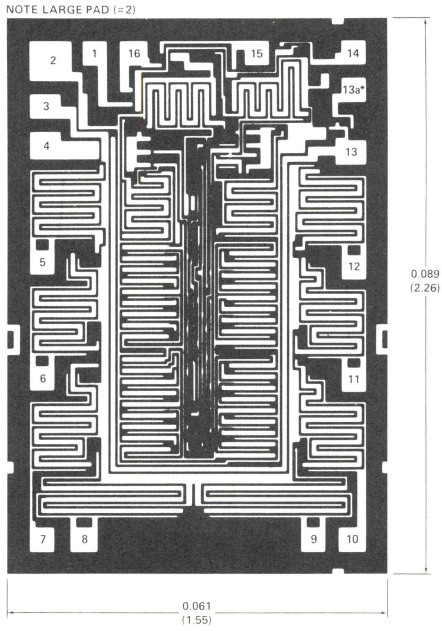


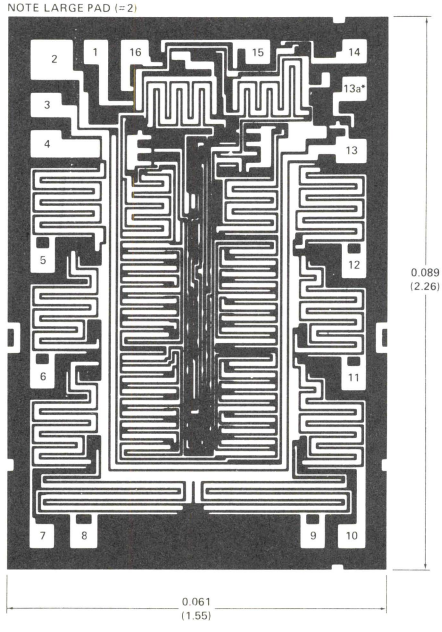
PIN NO.	FUNCTION
1	ENABLE
2†	V+ (SUBSTRATE)
3	DRAIN
4†	V+ (SUBSTRATE)
5	SOURCE 8
6	SOURCE 7
7	SOURCE 6
8	SOURCE 5
9	SOURCE 4
10	SOURCE 3
11	SOURCE 2
12	SOURCE 1
13	V–
14	ADDRESS 0
15	ADDRESS 1
16	ADDRESS 2

*13a is connected to V–

† Pins 2 and 4 are interconnected, either one may be used

Pin numbers are for dual in-line packages

DG501



PIN NO.	FUNCTION
1	ENABLE
2*	V+ (SUBSTRATE)
3	DRAIN
4*	V+ (SUBSTRATE)
5	SOURCE 8
6	SOURCE 7
7	SOURCE 6
8	SOURCE 5
9	SOURCE 4
10	SOURCE 3
11	SOURCE 2
12	SOURCE 1
13	V–
14	ADDRESS 0
15	ADDRESS 1
16	ADDRESS 2

*Pins 2 and 4 are interconnected, either one may be used

Pin numbers are for dual in-line packages

DG503

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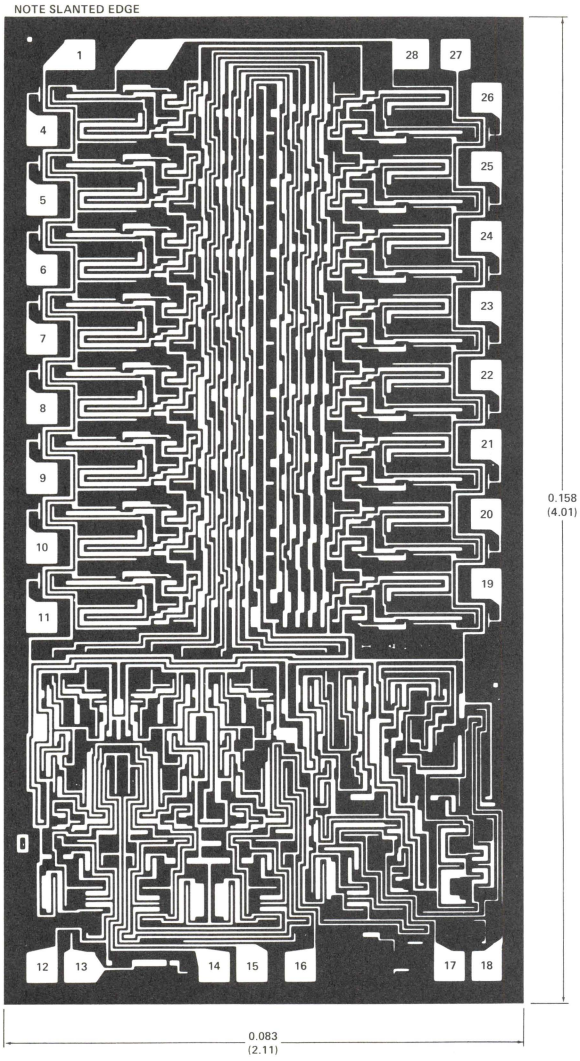

PIN NO.	FUNCTION
1	V+ (SUBSTRATE)
4	SOURCE 16
5	SOURCE 15
6	SOURCE 14
7	SOURCE 13
8	SOURCE 12
9	SOURCE 11
10	SOURCE 10
11	SOURCE 9
12	GROUND
13	V_{REF}
14	ADDRESS 3
15	ADDRESS 2
16	ADDRESS 1
17	ADDRESS 0
18	ENABLE
19	SOURCE 1
20	SOURCE 2
21	SOURCE 3
22	SOURCE 4
23	SOURCE 5
24	SOURCE 6
25	SOURCE 7
26	SOURCE 8
27	V–
28	DRAIN

Pin numbers are for dual in-line packages

DG506

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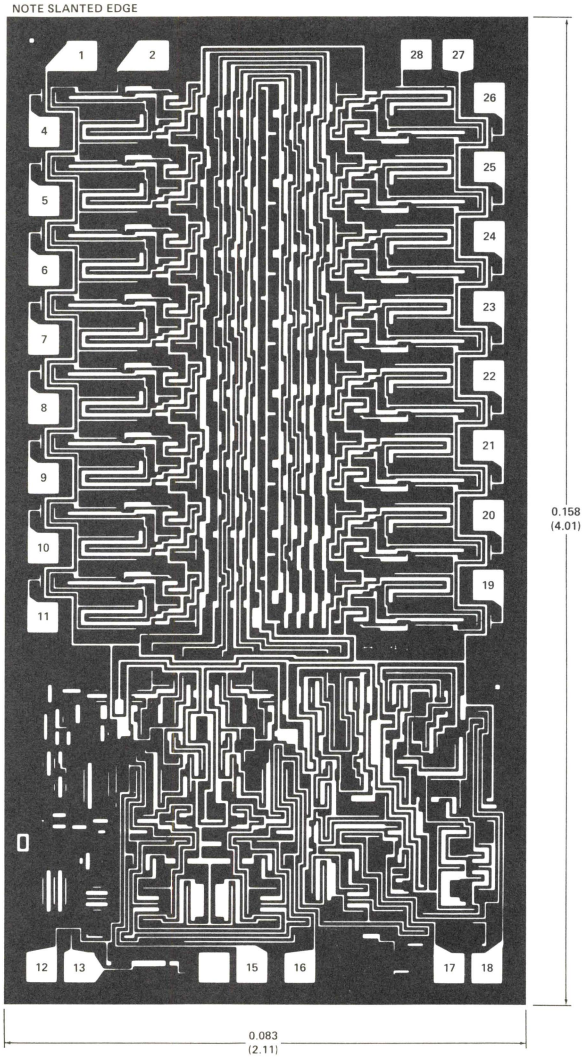

PIN NO.	FUNCTION
1	V+ (SUBSTRATE)
2	DRAIN b
4	SOURCE 8b
5	SOURCE 7b
6	SOURCE 6b
7	SOURCE 5b
8	SOURCE 4b
9	SOURCE 3b
10	SOURCE 2b
11	SOURCE 1b
12	GROUND
13	V_{REF}
15	ADDRESS 2
16	ADDRESS 1
17	ADDRESS 0
18	ENABLE
19	SOURCE 1a
20	SOURCE 2a
21	SOURCE 3a
22	SOURCE 4a
23	SOURCE 5a
24	SOURCE 6a
25	SOURCE 7a
26	SOURCE 8a
27	V−
28	DRAIN a

Pin numbers are for dual in-line packages

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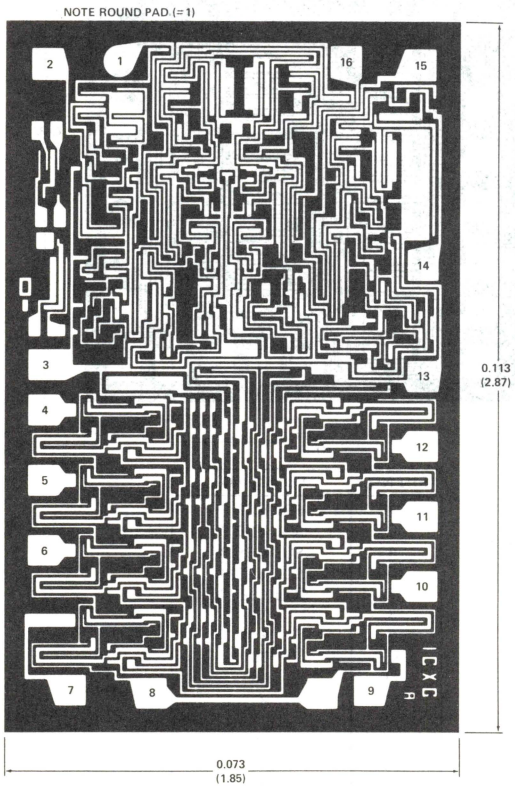
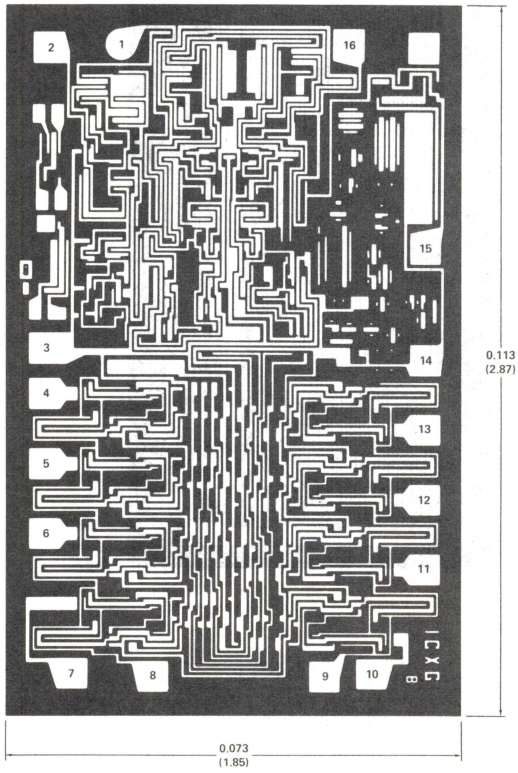


PIN NO.	FUNCTION
1	ADDRESS 0
2	ENABLE
3	V–
4	SOURCE 1
5	SOURCE 2
6	SOURCE 3
7	SOURCE 4
8	DRAIN
9	SOURCE 8
10	SOURCE 7
11	SOURCE 6
12	SOURCE 5
13	V+ (SUBSTRATE)
14	GROUND
15	ADDRESS 2
16	ADDRESS 1

Pin number are for dual in-line packages

DG508



PIN NO.	FUNCTION
1	ADDRESS 0
2	ENABLE
3	V–
4	SOURCE 1a
5	SOURCE 2a
6	SOURCE 3a
7	SOURCE 4a
8	DRAIN a
9	DRAIN b
10	SOURCE 4b
11	SOURCE 3b
12	SOURCE 2b
13	SOURCE 1b
14	V+ (SUBSTRATE)
15	GROUND
16	ADDRESS 1

Pin numbers are for dual in-line packages

DG509

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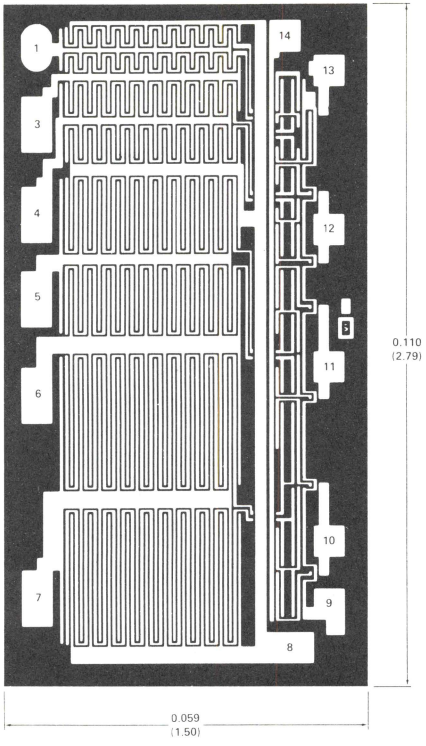
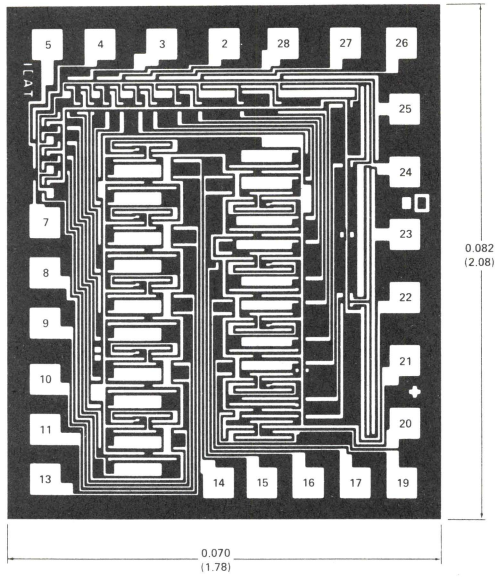
NOTE ROUND PAD (#1)



PIN NO.	FUNCTION
1	SOURCE 4
3	ANALOG GROUND 2
4	SOURCE 3
5	SOURCE 2
6	ANALOG GROUND 1
7	SOURCE 1
8	SUM JCT
9	V+ (SUBSTRATE)
10	B1
11	B2
12	B3
13	B4
14	V–

Pin numbers are for dual in-line packages

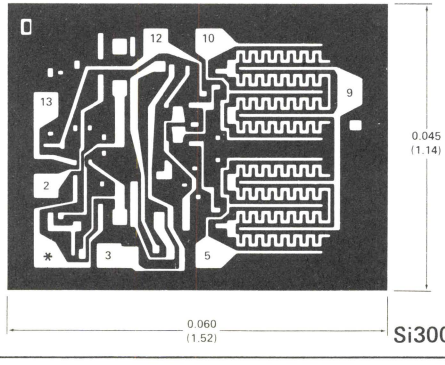
DG515



PIN NO.	FUNCTION
2	SOURCE 6
3	SOURCE 7
4	SOURCE 8
5	SOURCE 9
7	SOURCE 10
8	V–
9	B10
10	B9
11	B8
13	B7
14	B6
15	B5
16	B4
17	B3
19	B2
20	B1
21	V+ (SUBSTRATE)
22	SUM JCT
23	S1
24	ANALOG GROUND
25	S2
26	S3
27	S4
28	S5

Pin numbers are for dual in-line packages

DG516



Si3002

PIN NO.	FUNCTION
2	V_R
3	V– (SUBSTRATE)
5	SOURCE 1
9	DRAIN
10	SOURCE 2
12	V+
13	INPUT

Pin numbers are for dual in-line packages

*THIS PAD IS AN ALTERNATE FOR PAD 13 AS AN INPUT

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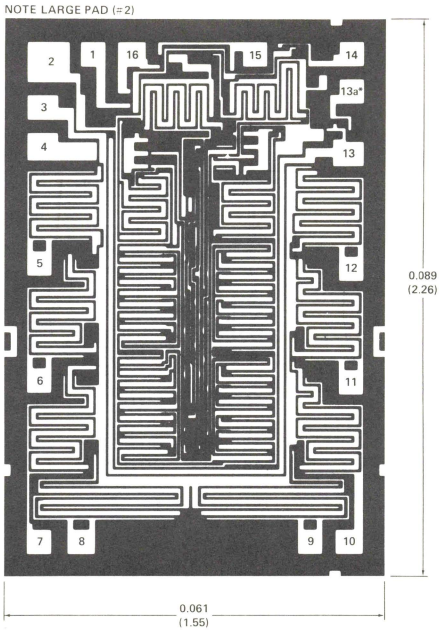
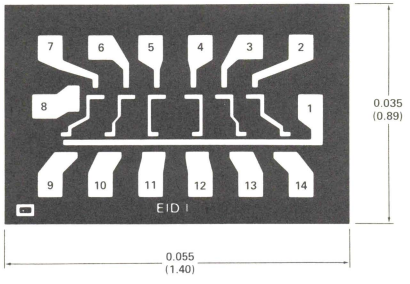


PIN NO.	FUNCTION
1	ENABLE
2	V+ (SUBSTRATE)
3	D
4	V+ (SUBSTRATE)
5	SOURCE 8
6	SOURCE 7
7	SOURCE 6
8	SOURCE 5
9	SOURCE 4
10	SOURCE 3
11	SOURCE 2
12	SOURCE 1
13	V–
14	ADDRESS 0
15	ADDRESS 1
16	ADDRESS 2

Pin numbers are for dual in-line packages

Both V+ pads are internally connected, either one or both may be used. V+ common to substrate.

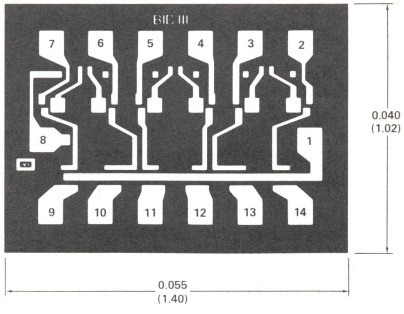
Si3705



PIN NO.	FUNCTION
1	V– (SUBSTRATE)
2	INPUT 1
3	INPUT 2
4	INPUT 3
5	INPUT 4
6	INPUT 5
7	INPUT 6
8	V_R
9	OUTPUT 6
10	OUTPUT 5
11	OUTPUT 4
12	OUTPUT 3
13	OUTPUT 2
14	OUTPUT 1

Pin numbers are for dual in-line packages

D123



PIN NO.	FUNCTION
1	V– (SUBSTRATE)
2	INPUT 1
3	INPUT 2
4	INPUT 3
5	INPUT 4
6	INPUT 5
7	INPUT 6
8	V_L
9	OUTPUT 6
10	OUTPUT 5
11	OUTPUT 4
12	OUTPUT 3
13	OUTPUT 2
14	OUTPUT 1

Pin numbers are for dual in-line packages

D125

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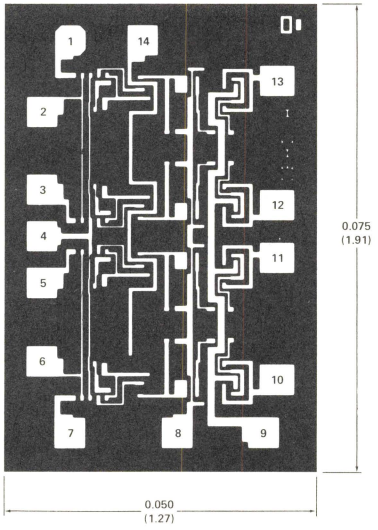
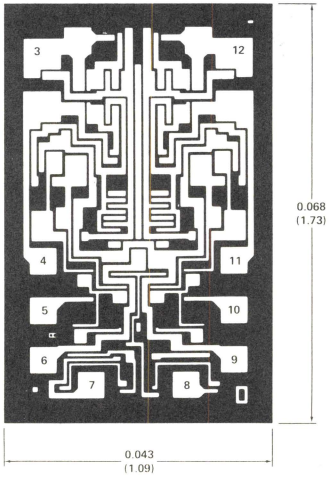


PIN NO.	FUNCTION
1	INPUT 1
2	INPUT 2
3	INPUT 3
4	INPUT 4
5	INPUT 5
6	INPUT 6
7	INPUT 7
8	V_R
9	V– (SUBSTRATE)
10	OUTPUT 4
11	OUTPUT 3
12	OUTPUT 2
13	OUTPUT 1
14	V_L

Pin numbers are for dual in line packages

D129



PIN NO.	FUNCTION
3	$\overline{\text{OUT 1}}$
4	OUT 1
5	INPUT 1
6	V+
7	V_L
8	V_R
9	V– (SUBSTRATE)
10	INPUT 2
11	OUT 2
12	$\overline{\text{OUT 2}}$

Pin numbers are for dual in-line packages

D139

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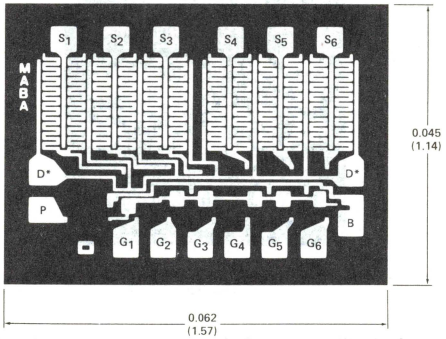

*Both "D" pads are electrically common. Either can be used for drain contact.

PAD	G115 DUAL IN-LINE PACKAGE PIN NO.	G116 DUAL IN-LINE PACKAGE PIN NO.	G117 FLAT PACK PIN NO.	G118 DUAL IN-LINE PACKAGE PIN NO.	G124 DUAL IN-LINE PACKAGE PIN NO.	FUNCTION
†G_1	2	2	3	1	2	GATE 1
†G_2	3	3	4	2	3	GATE 2
†G_3	4	4	5	3	4	GATE 3
†G_4	5	5	6	4	5	GATE 4
†G_5	6	6	7	5	NOT USED	GATE 5
†G_6	7	NOT USED	2	6	NOT USED	GATE 6
B	9	8	8	7	8	BODY (SUBSTRATE) V+
D	16	14	NOT USED	8	14	DRAIN
S_6	10	NOT USED	14**	9	NOT USED	SOURCE 6
S_5	11	9	9	10	NOT USED	SOURCE 5
S_4	12	10	10	11	10	SOURCE 4
S_3	13	11	11	12	11	SOURCE 3
S_2	14	12	12	13	12	SOURCE 2
S_1	15	13	13	14	13	SOURCE 1
P	1	1	1	TIED TO SUBSTRATE	1	PULL UP GATE INPUT

†Any unused gates should be connected to the substrate V+; unused sources can be left open

** The G117 uses the S_6 pad as the drain output (pin 14 on package).

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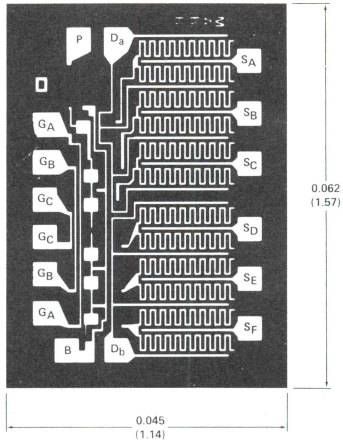
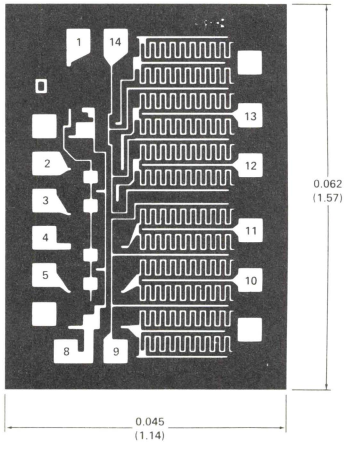


PAD	G119		G122	
	FLAT PACK PIN NO.	FUNCTION	FLAT PACK PIN NO.	FUNCTION
G_a	3	GATE 1	3	GATE 2
G_b	4	GATE 3		
G_c	5	GATE 5	†NOT USED	
G_c				
G_b			5	GATE 1
G_a				
B	6	BODY (SUBSTRATE V+)	8	BODY (SUBSTRATE V+)
D_b	7	DRAIN 2	9	DRAIN 1
S_F	9	SOURCE 2	10	SOURCE 1
S_E	10	SOURCE 4	11	SOURCE 2
S_D	11	SOURCE 6	NOT USED	
S_C	12	SOURCE 5	NOT USED	
S_B	13	SOURCE 3	12	SOURCE 3
S_A	14	SOURCE 1	13	SOURCE 4
D_a	1	DRAIN 1	14	DRAIN 2
P	2	PULL UP GATE INPUT	1	PULL UP GATE INPUT

†Any unused gates should be connected to the substrate V+; unused sources can be left open.

G119
G122



PIN NO.	FUNCTION
1	P (PULL UP GATE INPUT)
2	GATE 1
3	GATE 2
4	GATE 3
5	GATE 4
8	BODY (SUBSTRATE) V+
9	DRAIN 2
10	SOURCE 4
11	SOURCE 3
12	SOURCE 2
13	SOURCE 1
14	DRAIN 1

Pin numbers are for dual in-line packages.

G123

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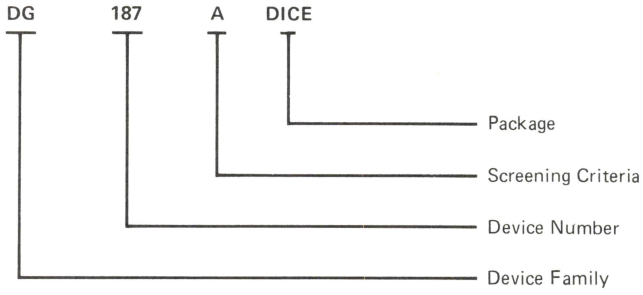
Die Ordering Information



DIE FAMILY
(1, 2 or 3 Letters)

D – Drivers for FET Switches
DG – Analog Switches
DGM – Analog Switches
G – Multi-Channel FETs
Si – Siliconix Second Source Part

DEVICE NUMBER
(3 or 4 Digit Numbers)

SCREENING CRITERIA
(1 Letter)

A – Electrically probed @ 25°C to "A" Suffix of respective data sheet; visual criteria screening to MIL-STD-883, Method 2010 Condition B.

I – Electrically probed @ 25°C to "C" Suffix of respective data sheet; visual criteria screening to Siliconix Specification 5018.

PACKAGE
(4 Letters)

DICE – Chips waffle packed per Figure 4 in Die Process Information

OTHER OPTIONS

SEM, wafer qualification should be specified as a separate line item on a request for quote.

Options for Die-In-Wafer form goldbacking, Class A visual, to customer visual criteria are considered "special" and a special part number will be assigned. Please identify as "Similar to _____ with the following additional conditions _____."

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Burn In Pin Connections

The following table lists the standard Burn-In Pin Connections for most Siliconix Analog Switches. Devices are listed in Alpha-Numerical order according to package type. Following the tables are two examples illustrating Burn-In Pin Connections for different switches and packages.

Burn In Pin Connections

The following table lists the standard Burn-In Pin Connections for most Siliconix Analog Switches. Devices are listed in Alpha-Numerical order according to package type. Following the tables are two examples illustrating Burn-In Pin Connections for different switches and packages.

Part Type	Package Type	Pins															
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DGM111	P/L	–	GND	–	–20 V	–	GND	–	10K→ –20 V	+5 V	+5 V	+5 V	GND	–	GND		
DG123	P/L	GND	GND	GND	–20 V	4.7K→ +5 V	4.7K→ +5 V	4.7K→ +5 V	4.7K→ +5 V	4.7K→ +5 V	GND	+5 V	GND	GND	GND		
DG125	P/L	GND	GND	GND	–20 V	GND	GND	GND	GND	GND	+5 V	+5 V	GND	GND	GND		
DG126 DG129 DG133 DG134 DG139 DG140 DG141 DG142 DG143 DG144 DG145 DG146 DG151 DG152 DG153 DG154 DG161 DG162 DG163 DG164	P/L	10K→ GND	+10 V	10K→ GND	–	+10 V	10K→ GND	10K→ GND	+10 V	GND	GND	+10 V	–20 V	GND	+10 V		
DG172	P/L	To Pin 14	GND	GND	–	–20 V	GND	+5 V	+5 V	+5 V	+5 V	GND	+5 V	To Pin 14	7.5K→ –20 V		

Parentheses indicate direct connection to indicated pin i.e. (2) = connect to pin 2; All voltages ±5%; Package types: P = All Dual-In-Line Packages, L = All Flat Packages, A = All 10-Lead TO-5's, R = 28-Pin Dual-In-Line Packages.

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Burn-In Pin Connections (Continued)

Part Type	Package Type	Pins 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DG180 DG181 DG182 DG186 DG187 DG188 DG281	A	+15 V	10K→ GND	GND	+15 V	+5 V	GND	−15 V	GND	10K→ GND	+15 V						
DG180 DG181 DG182 DG281	P/L	+15 V	10K→ GND	–	–	GND	+15 V	+5 V	GND	−15 V	GND	–	–	10K→ GND	+15 V		
DG183 DG184 DG185 DG189 DG190 DG191 DG284 DG290	P	10K→ GND	–	10K→ GND	−15 V	−15 V	10K→ GND	–	10K→ GND	+15 V	GND	+15 V	+5 V	GND	−15 V	GND	+15 V
DG183 DG184 DG185 DG186 DG187 DG188 DG189 DG190 DG191 DG284 DG290	L	−15 V	10K→ GND	10K→ GND	+15 V	GND	+15 V	+5 V	GND	−15 V	GND	+15 V	10K→ GND	10K→ GND	−15 V		
DG200	A	+15 V	+15 V	GND	(9)	(9)	−15 V	–	(9)	10K→ GND	+15 V						
	P/L	+15 V	–	GND	–	(10)	(10)	−15 V	–	(10)	10K→ GND	–	+15 V	–	+15 V		
DG201	P/L	+15 V	(15)	(15)	−15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	–	+15 V	(15)	10K→ GND	+15 V

Parentheses indicate direct connection to indicated pin i.e. (2) = connect to pin 2; All voltages ±5%; Package types: P = All Dual-In-Line Packages, L = All Flat Packages, A = All 10-Lead TO-5's, R = 28-Pin Dual-In-Line Packages.

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Burn-In Pin Connections (Continued)

Part Type	Package Type	Pins 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DG300 DG301 DG304 DG305	A	(9)	(9)	GND	–	GND	–15 V	GND	(9)	10K→ GND	+15 V						
DG300 DG301 DG302 DG303 DG304 DG305 DG306 DG307	P/L	–	(13)	(13)	(13)	(13)	GND	GND	–15 V	GND	(13)	(13)	(13)	10K→ GND	+15 V		
DG381	A/P	See DG181															
DG384	A/P	See DG184															
DG387	A/P	See DG187															
DG390	A/P	See DG190															
DG501 DG503 SI3705	P/L	(16)	+15 V	(13)	+15 V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	1K→ –20 V	(16)	(16)	10K→ –15 V
DG506 DG507	R	**1** +15 V	**2** (28)	**3** –	**4** (28)	**5** (28)	**6** (28)	**7** (28)	**8** (28)	**9** (28)	**10** (28)	**11** (28)	**12** GND	**13** –	**14** GND	**28 Pins**	
		15 GND	**16** GND	**17** GND	**18** GND	**19** (28)	**20** (28)	**21** (28)	**22** (28)	**23** (28)	**24** (28)	**25** (28)	**26** (28)	**27** –15 V	**28** 10K→ GND		
DG508	P/L	GND	GND	–15 V	(12)	(12)	(12)	(12)	(12)	(12)	(12)	(12)	10K→ GND	+15 V	GND	GND	GND
DG509	P/L	GND	GND	–15 V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10K→ GND	+15 V	GND	GND
D139	P/L	–	–	10K→ Pin 4	10K→ Pin 3	+5 V	+10 V	+5 V	GND	–20 V	GND	10K→ Pin 12	10K→ Pin 11	–	–		

Parentheses indicate direct connection to indicated pin i.e. (2) = connect to pin 2; All voltages ±5%; Package types: P = All Dual-In-Line Packages, L = All Flat Packages, A = All 10-Lead TO-5's, R = 28-Pin Dual-In-Line Packages.

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Burn In Pin Connections (Continued)

Part Type	Package Type	Pins															
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
D129	P/L	(7)	(7)	(7)	GND	(7)	(7)	10K→ +5 V	GND	−30 V	(13)	(13)	(13)	10K→ +5 V	+5 V		
D123/ D125	P/L	−30 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ GND		
G115	P/L	(16)	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(16)	(16)	(16)	(16)	(16)	(16)	(16)	(16)	10K→ +10 V
G116	P/L	(14)	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V		
G118	P/L	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V		
G119	P/L	(14)	(14)	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V		
G122	P/L	(14)	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V		
G123	P/L	(14)	−15 V	−15 V	−15 V	−15 V	−15 V	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	10K→ +10 V		

Parentheses indicate direct connection to indicated pin i.e. (2) = connect to pin 2; All voltages ±5%; Package types: P = All Dual-In-Line Packages, L = All Flat Packages, A = All 10-Lead TO-5's, R = 28-Pin Dual-In-Line Packages.

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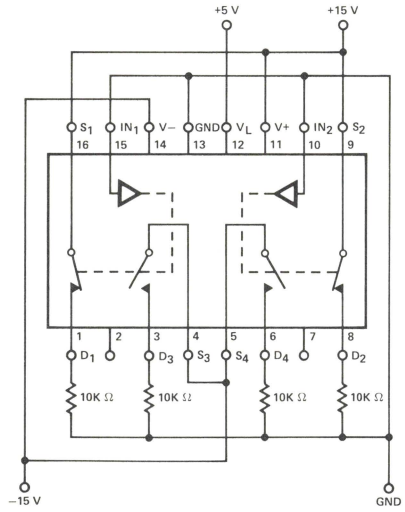
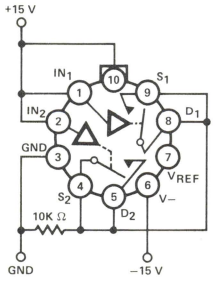
Burn-In Pin Connections (Continued)

Examples of Burn-In Circuit Configurations



DG190/DG191 (PACKAGE TYPE P)



DG200 (PACKAGE TYPE A)

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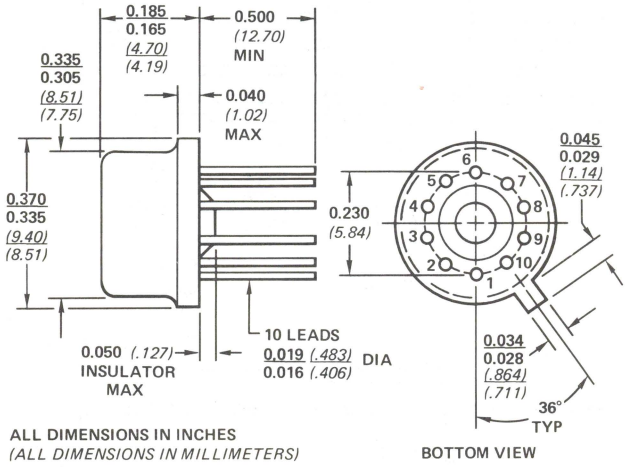
Analog Switches 1
Drivers for FET Switches 2
Multi-Channel FETs 3
Die Process and Topography Information 4
Burn-In Pin Connections 5
Mechanical Data 6
Appendices 7



PACKAGE 2
10 LEAD TO-100 TYPE METAL CAN **(A)**

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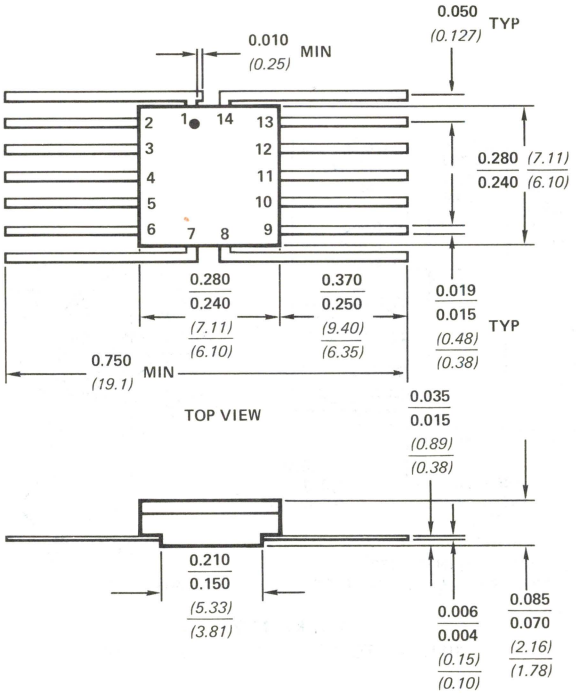

PACKAGE 5
14 LEAD FLATPAC (L)
(BOTTOM BRAZE)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

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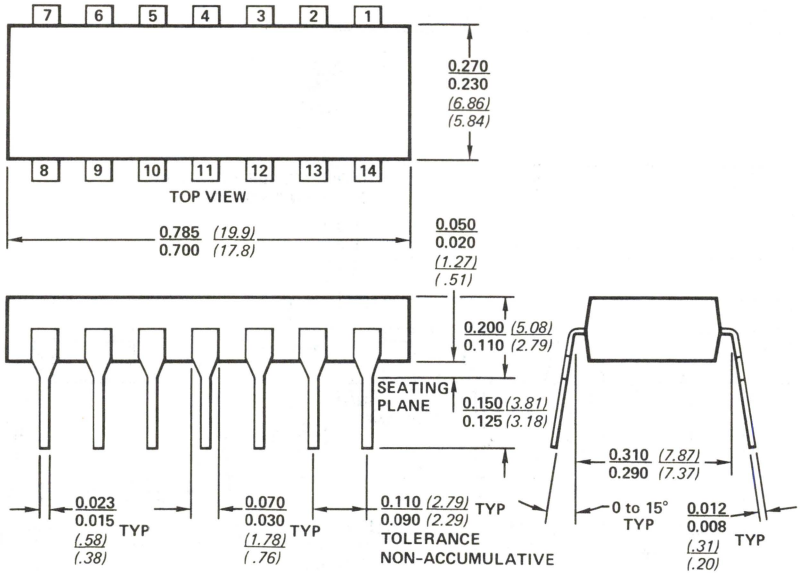
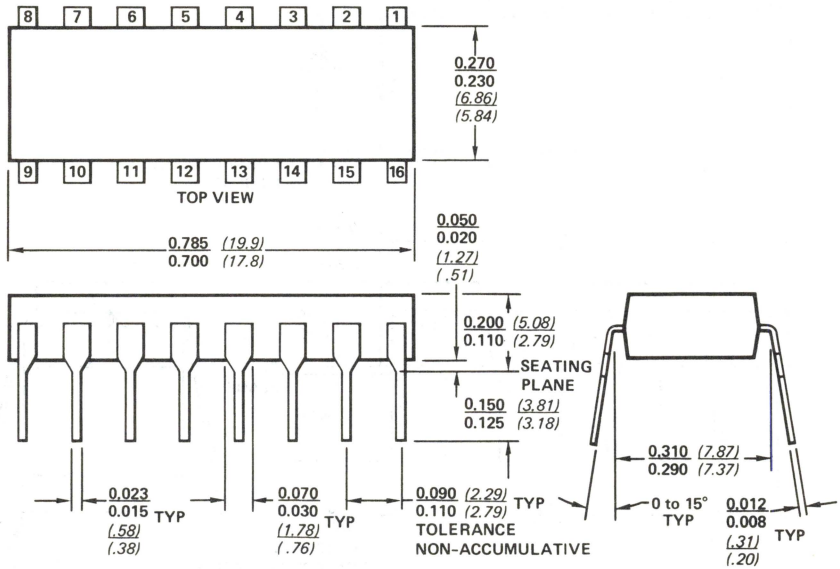


PACKAGE 7
14 LEAD DUAL IN LINE PACKAGE (J)
(PLASTIC)



PACKAGE 8
16 LEAD DUAL IN LINE PACKAGE(J)
(PLASTIC)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

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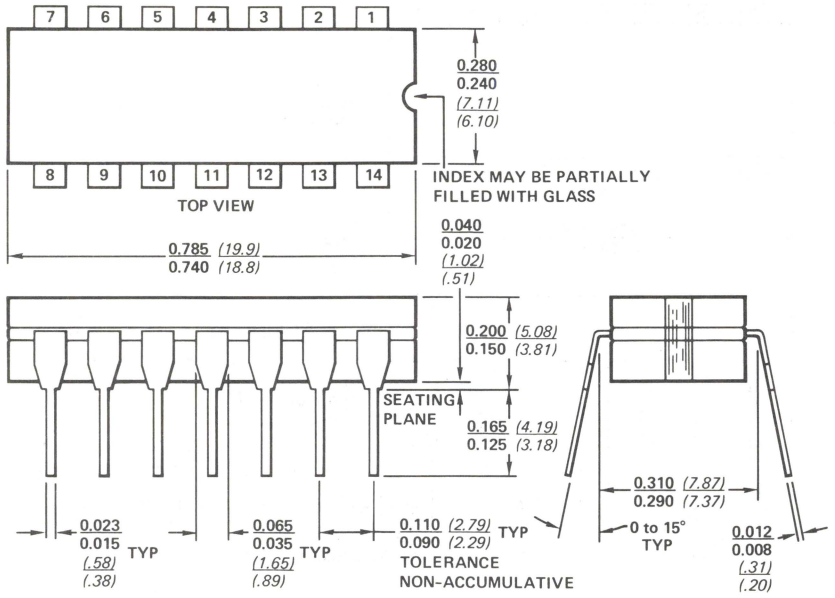
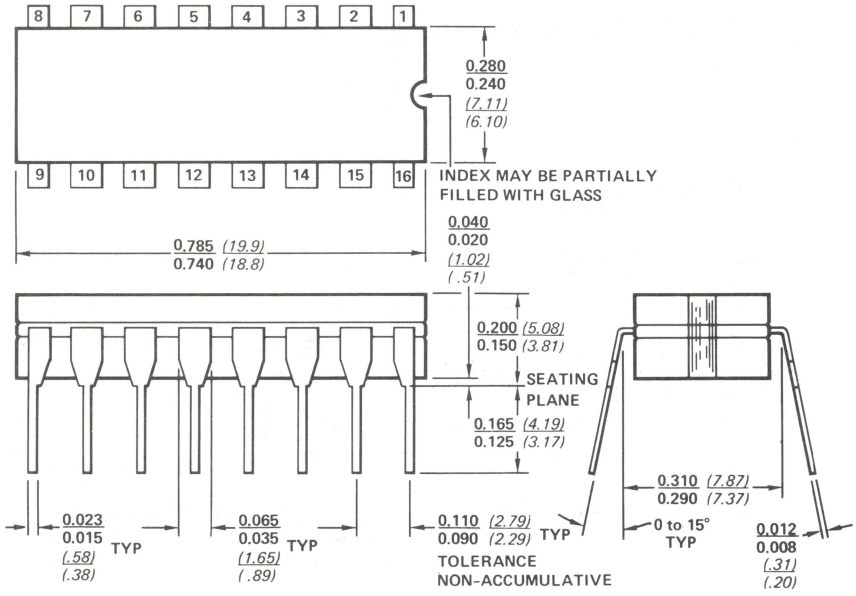


PACKAGE 9
14 LEAD DUAL IN LINE PACKAGE (K)
(CERDIP)



PACKAGE 10
16 LEAD DUAL IN LINE PACKAGE (K)
(CERDIP)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

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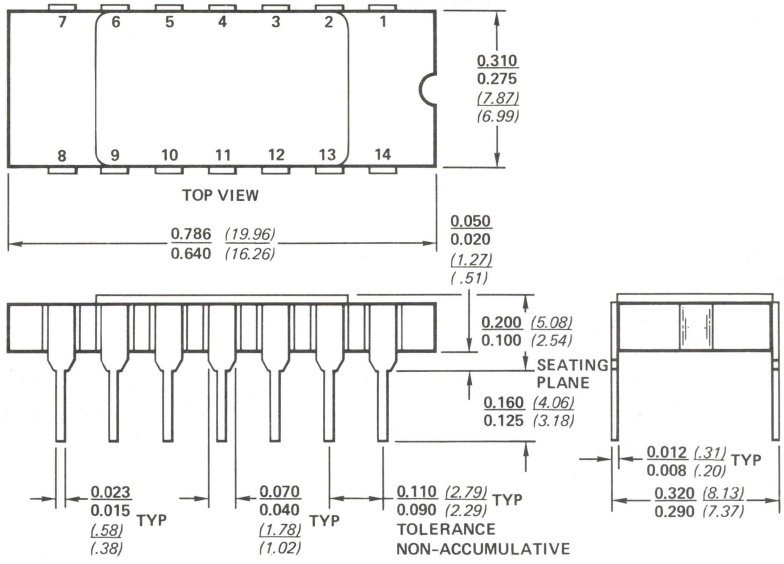
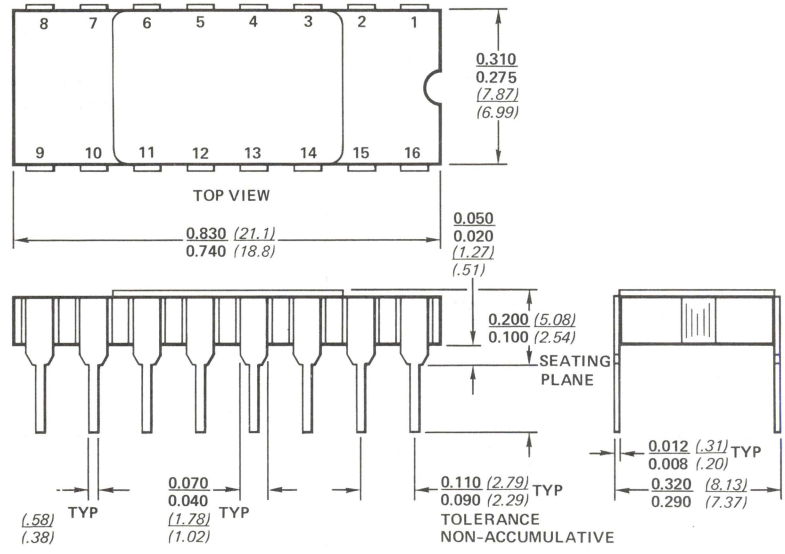


PACKAGE 11
14 LEAD DUAL IN LINE PACKAGE (P)
(SIDE BRAZE)



PACKAGE 12
16 LEAD DUAL IN LINE PACKAGE (P)
(SIDE BRAZE)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

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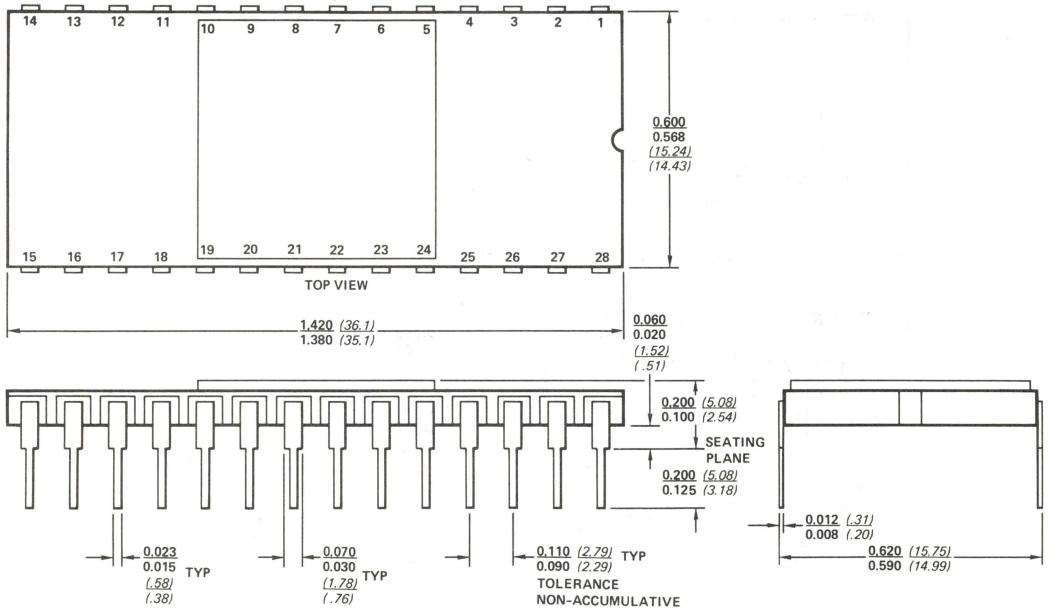
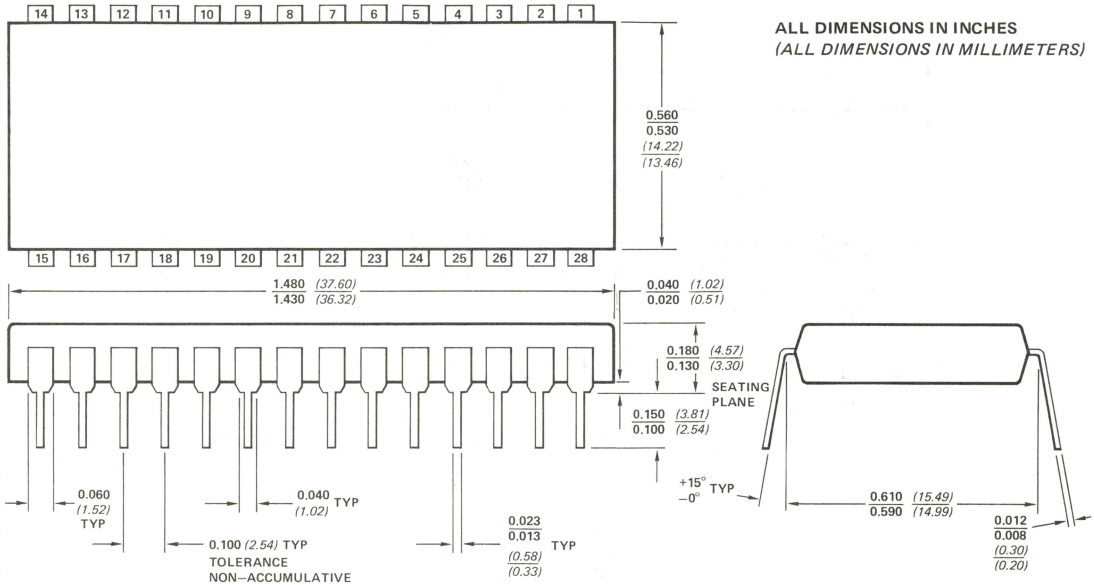


PACKAGE 13
28 LEAD DUAL IN LINE PACKAGE (R)
(SIDE BRAZE)



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

PACKAGE 14
28 LEAD DUAL IN-LINE PACKAGE (J)
(PLASTIC)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

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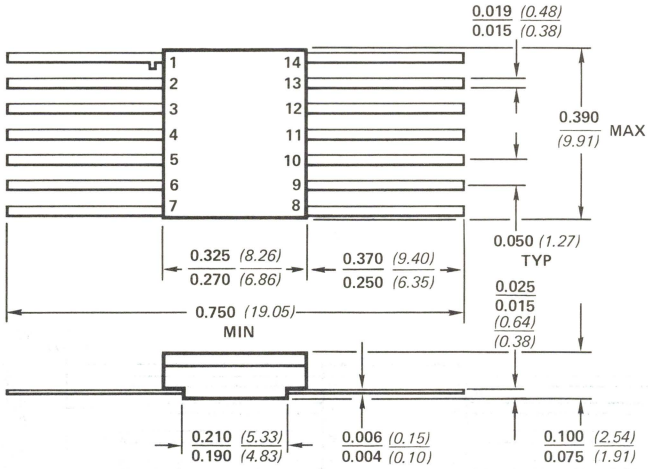
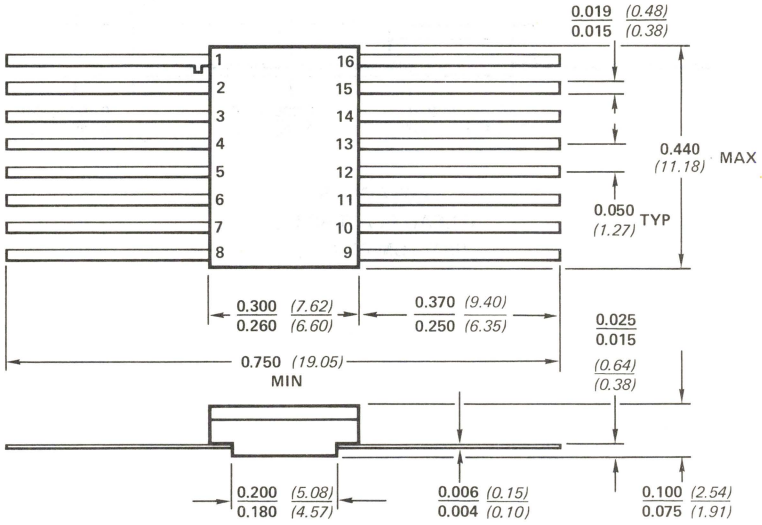


PACKAGE 16
14 LEAD FLATPAC (L)
(BOTTOM BRAZE)



PACKAGE 17
16 LEAD FLATPAC (L)
(BOTTOM BRAZE)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

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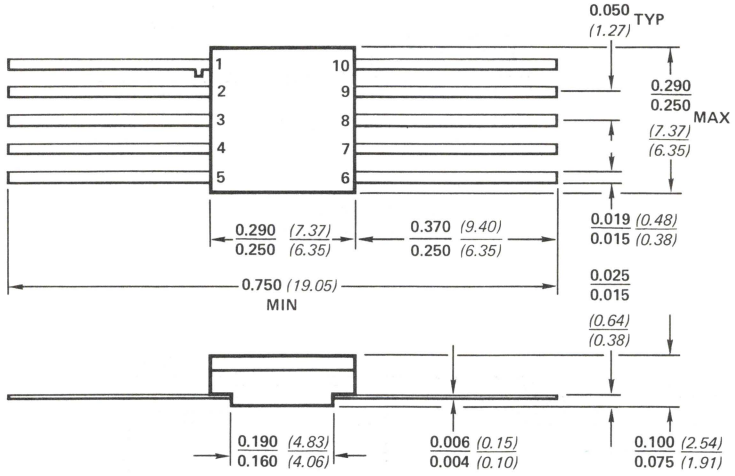

PACKAGE 18
10 LEAD FLATPAC (L)
(BOTTOM BRAZE)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP AND/OR BOTTOM OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

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Analog Switches 1
Drivers for FET Switches 2
Multi-Channel FETs 3
Die Process and Topography Information 4
Burn-In Pin Connections 5
Mechanical Data 6
Appendices 7

Publications Index

Catalog (See Key)	Document Number	Title
		Application Notes
	AN70-1	FET Cascode Circuits Reduce Feedback Capacitance
F	AN70-2	FETs for Video Amplifiers
	AN71-1	A High Resolution CMRR Test Method
F	AN72-1	FETs in Balanced Mixers
A	AN72-2	FETs as Analog Switches
F	AN73-1	FETs as Voltage-Controlled Resistors
A	AN73-2	IC Multiplexer Increases Analog Switching Speeds
A	AN73-3	Switching High-Frequency Signals With FET Integrated Circuits
	AN73-4	Junction FETs in Active Double-Balanced Mixers
A	AN73-5	Driver Circuits for the JFET Analog Switch
L	AN73-6	Function/Application of the L144 Programmable Micro-Power Triple Op Amp
F, A	AN73-7	An Introduction to FETs
L	AN74-1	Function/Application of the LD110/LD111 3½ Digit A/D Converter Set
A	AN74-2	Analog Switches in Sample and Hold Circuits
	AN74-3	Designing Junction FET Input Op Amps
F	AN74-4	Audio-Frequency Noise Characteristics of Junction FETs
A	* AN75-1	CMOS Analog Switches—A Powerful Design Tool
	AN76-1	Measuring High Frequency S-Parameters on the Dual Gate MOSFET
VA	AN76-3	VMOS—A Breakthrough in Power MOSFET Technology
L	* AN76-4	Function/Application of the LD110/LD114 3½ Digit A/D Converter Set
L	AN76-5	Function/Application of the LD130 ±3 Digit Converter
A	* AN76-6	DG300 Series Analog Switch Applications
L	* AN76-7	Function/Application of the L161 Industry's First Programmable Micro-power Comparator
L	* AN77-1	Function/Application of the LD120/LD121 4½ Digit A/D Converter Set in Measurement Systems
F, VA	* AN77-2	Don't Trade Off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches
L	* AN77-3	Function/Application of the LD120/LD121 4½ Digit A/D Converter Interfaced with an 8080A Microprocessor
T	* AN77-4	Function/Application of the DF331/DF332 New Companding Converter Chip Set
VA	* AN79-1	A 500 KHz Switching Inverter for 12 V Systems
VA	* AN79-3	Dynamic Input Characteristics of a VMOS Power Switch
F, VA	* AN79-4	Driving VMOS Power FETs
	AN79-5	Using the VN64GA High Current, High Power VMOS Power FET
VA	* AN79-6	Using VMOS Transistors to Interface from IC Logic to High Power Loads
	AN79-7	Applications of the VN10KM VMOS Power FET
VA	* AN80-1	A Key to the Advance of Switching Power Supplies
VA	* AN80-2	Meet the VMOS FET Model
	AN80-3	Ultralinear Broadband Amplifier
	AN80-4	Enjoy VHF Power Amplifier Design
VA	* AN80-5	An Alternative Power Amplifier Design
		Design Aids
L	DA74-1	Design Aid of the LD110/LD111 3½ Digit DVM Demonstrator Board
L	DA76-2	Design Aid of the LD130 ±3 Digit DVM Demonstrator Board
L	DA76-3	Design Aid of the LD130 ±3 Digit Auto-Ranging DMM
L	DA77-1	Design Aid to Build a Portable 0 to 99.9°F LCD Display Thermometer Using the DF411
L	DA77-2	Design Aid of the LD120/LD121 4½ Digit DVM
T	* DA78-1	Design Aid to Build a CODEC Evaluation Demonstrator with the DF331/DF332/DF334
T	* DA78-2	Considerations for the Filtering of Analog Signals in DF331/DF332/DF334 CODEC Converter Applications
VA	* DA80-1	A Low Cost Regulator for Microprocessor Applications

Key

Catalogs

A = Analog Switches and Their Applications
F = FET Design Catalog
L = LSI Data Book
T = Telecommunications Data Book
VA = VMOS Applications Handbook

*Available in bound catalog only.

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Publications Index (Cont'd)

Catalog (See Key)	Document Number	Title
		Design Ideas
F	DI71-1	The FET Constant Current Source
	DI71-4	Wideband Mixer-Preamplifier Using FETs
	DI71-5	A FET Frequency Doubler
	DI71-6	Using FETs in Selective VHF Amplifiers
	DI71-8	Using JFETs in Ultra-Wideband UHF Amplifiers
F	DI71-9	Wideband UHF Amplifier with High Performance FETs
F	DI73-2	High Performance FETs in Low-Noise VHF Oscillators
		Technical Articles
	TA70-1	High Frequency Junction FET Characterization and Application
F	TA70-2	FET Biasing
A	TA73-1	Multiplexer Adds Efficiency to 32-Channel Telephone System
A	TA73-2	Designing with Monolithic FET Switches
	TA76-1	VMOS Power FETs in Your Next Broadband Driver
	TA76-2	A New Technology: Application of VMOS Power FETs for High Frequency Communications
T	* TA78-1	Designing with CODECs: Know Your A's and μ's
VA	* TA78-2	Designing a VMOS 250 Watt Off-Line Inverter
T	* TA79-1	CODEC Has On-Chip Signaling for Phone Applications

Catalogs

Analog Switch Data Book

Analog Switches and Their Applications ($7.95 charge)

FET Design Catalog

LSI Data Book

Telecommunications Data Book

VMOS Power FETs Design Catalog

VMOS Power FETs Applications Handbook

OEM Pricing/Product Information Selector Guide

Title

Reprints & Reports

Designing a VMOS 250 Watt Off-Line Inverter. David C. Hoffman, *Powercon* 3/78

Designing with CODECs: Know Your A's and μ's. Thomas J. Mroz, *EDN* 5/76

Log Data under μ Control. Gary Grandbois, *Electronic Design* 5/76

Higher Power Ratings Extend VMOS FETs' Dominion. Arthur D. Evans, David C. Hoffman, Edwin S. Oxner, Walter Heinzer and Lee Shaeffer. *Electronics* 6/78

Siliconix, Inc. Annual Report.

CODEC has On-Chip Signaling for Phone Applications, Walter Heinzer and Steve Bolger, *Electronics* 6/7/79

A Microprocessor Controlled VMOS Power Supply, David C. Hoffman

Control Analog Signals with Voltage, Stephen Moore, *Electronic Design,* 1978

Exploit VMOS FETs' Advantages to Drive Bipolar Power Transistors, F. Michael Barlage, *Powercon* 5/78

Key

Catalogs

A = Analog Switches and Their Applications

F = FET Design Catalog

L = LSI Data Book

T = Telecommunications Data Book

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Glossary of Terms and Abbreviations

Siliconix

A_0, A_1, A_2, A_3
A^0, A^1, A^2, A^3 = Address Inputs

A_{VOL} = D.C. Open Loop Voltage Gain

B = Body

BV_{DSS} = Drain-Source Breakdown Voltage

BV_{GBS} = Gate-Body Breakdown Voltage

BV_{GSS} = Gate-Source (Channel) Breakdown Voltage

BV_{PBS} = Pull-Up Gate-Body Breakdown Voltage

BV_{SDS} = Source-Drain Breakdown Voltage

C_{db} = Drain-Body Capacitance

$C_{D(off)}$ = Drain OFF Capacitance

$C_{D(on)} + C_{S(on)}$ = Channel ON Capacitance

$C_{ds(off)}$ = Drain-Source OFF Capacitance

C_{gb} = Gate-Body Capacitance

C_{gd} = Gate-Drain Capacitance

$C_{gd(off)} + C_{gs(off)}$ = Gate-Channel OFF Capacitance

$C_{gd(on)} + C_{gs(on)}$ = Gate-Channel ON Capacitance

C_{gs} = Gate-Source Capacitance

C_{IN} = Logic Input Capacitance

C_L = Load Capacitance

CMRR = Common Mode Rejection Ratio

C_{sb} = Source-Body Capacitance

$C_{S(off)}$ = Source OFF Capacitance

D = Drain

E_n = Enable Input

G = Gate

I_A = Address Input Current

$I_{A(peak)}$ = Peak Address Input Current

I_{AH} = Address Input Current, Input Voltage High

I_{AL} = Address Input Current, Input Voltage Low

I_{BIAS} = Input Bias Current

I_{H^+} = Positive Supply Current, Input Voltage High

I_{L^+} = Positive Supply Current, Input Voltage Low

I_D = Drain Current

$I_{D(off)}$ = Drain OFF Leakage Current

$I_{D(on)}$ = Drain ON Leakage Current

$I_{D(on)} + I_{S(on)}$ = Channel ON Leakage Current

I_{DSS} = Drain Current at Zero Gate Voltage

I_{H^-} = Negative Supply Current, Input Voltage High

I_{L^-} = Negative Supply Current, Input Voltage Low

I_{GBS} = Gate-Body Leakage Current

I_G = Gate Current

$I_{G(on)}$ = Gate ON Current

I_{GSS} = Gate-Channel Leakage Current

I_{IN} = Input Current

I_{INH} = Input Current, Input Voltage High

I_{INL} = Input Current, Input Voltage Low

I_L = Logic Supply Current

I_{LH} = Logic Supply Current, Input Voltage High

I_{LL} = Logic Supply Current, Input Voltage Low

I_{OH} = Output Current, High

I_{OL} = Output Current, Low

I_{OS} = Input Offset Current

I_P = Pull-Up Gate Current

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I_R	=	Reference Supply Current
I_{RH}	=	Reference Supply Current, Input Voltage High
I_{RL}	=	Reference Supply Current, Input Voltage Low
I_S	=	Source Current
I_{SC}	=	Short Circuit Output Current
$I_{S(off)}$	=	Source OFF Leakage Current
$I+$	=	Positive Supply Current
$I-$	=	Negative Supply Current
NC	=	No Connection
OC	=	Open Collector Logic
P	=	Pull-Up Gate
P_D	=	Power Dissipation
$r_{DS(on)}$	=	Drain-Source ON Resistance (D.C. measurement)
$\Delta r_{DS(on)}$	=	Fractional Change in Drain-Source ON Resistance (D.C. measurement)
R_{in}	=	Input Resistance
R_L	=	Load Resistance
S	=	Source
S_r	=	Slew Rate
T_A	=	Ambient Temperature
t_{off}	=	Turn-Off Time
$t_{off(En)}$	=	Enable Turn-Off Time
t_{on}	=	Turn-On Time
$t_{on(En)}$	=	Enable Turn-On Time
t_{open}	=	Break-Before-Make Interval
$t_{transition}$	=	Switching Time of Multiplexer
V_A	=	Address Input Voltage
V_{AH}	=	Address Input Voltage, High
V_{AL}	=	Address Input Voltage, Low
V_B	=	Body Voltage
V_D	=	Drain Voltage
V_{DB}	=	Drain-Body Voltage
V_{En}	=	Enable Input Voltage
V_G	=	Gate Voltage
V_{GB}	=	Gate-Body Voltage
V_{GD}	=	Gate-Drain Voltage
V_{GS}	=	Gate-Source Voltage
$V_{GS(off)}$	=	Gate-Source Pinchoff Voltage
$V_{GS(th)}$	=	Gate-Source Threshold Voltage
V_{IN}	=	Input Voltage
V_{INH}	=	Input Voltage, High
V_{INL}	=	Input Voltage, Low
V_L	=	Logic Supply Voltage
V_O	=	Output Voltage
V_{OH}	=	Output Voltage, High
V_{OL}	=	Output Voltage, Low
V_{OS}	=	Offset Voltage
V_{OUT}	=	Output Voltage
V_P	=	Pull-Up Gate Voltage
V_{PB}	=	Pull-Up Gate to Body Voltage
V_R	=	Reference Voltage
V_{REF}	=	Threshold Reference Voltage
V_S	=	Source Voltage
V_{SB}	=	Source-Body Voltage
V+	=	Positive Supply Voltage
V–	=	Negative Supply Voltage

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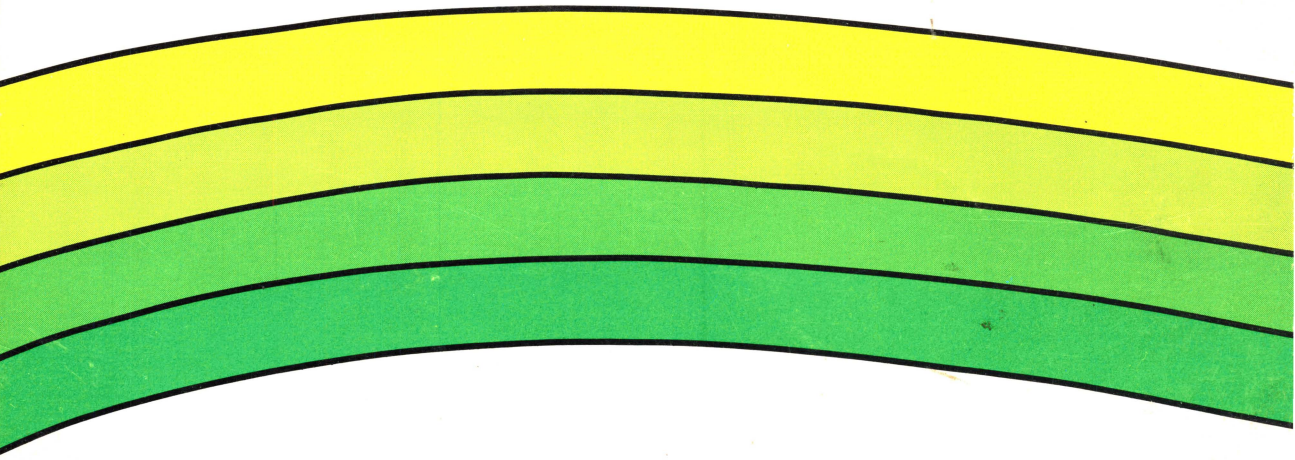
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